Active **N-PATH FILTER**

Theory and Design

Milad Darvishi

ACTIVE N-PATH FILTERS:
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Milad Darvishi

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Active N-path Filters: Theory and Design

DISSERTATION

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To Moloud and my parents

Samenvatting

Radio-ontvangers hebben te maken met sterke signalen buiten de ontvangstband, welke bandfilters noodzakelijk maken. Op dit moment kan het grootste gedeelte van zendontvangers op chip geïntegreerd worden, maar ondanks tientallen jaren onderzoek is het nog steeds niet mogelijk kwalitatief goede banddoorlaatfilters mee te integreren. De lage kwaliteit van geïntegreerde spoelen zorgt voor filters met grote verliezen, een klein dynamisch bereik en lage onderdrukking in de stopband. Om deze redenen gebruiken de meeste draadloze systemen tegenwoordig discrete filters naast de chip, wat hogere kosten en een groter volume met zich meebrengt. Dit wordt verergerd doordat moderne draadloze apparatuur vaak vele draadloze standaarden moet ondersteunen, hetgeen tot een veelheid aan externe filters leidt.

Banddoorlaatfilters gebaseerd op G_m-C filters en op LC filters met verbeterde kwaliteitsfactor zijn niet in staat goede specificaties te combineren met een grote verstembaarheid. N-path filters, daarentegen, bieden deze mogelijkheid wel doordat de frequentie van de doorlaatband wordt bepaald door een klokfrequentie en de bandbreedte door de waarde van capaciteiten. N-path filters zijn opgebouwd uit voornamelijk schakelaars, capaciteiten en digitale elektronica. Hierdoor kunnen ze uitstekend in CMOS processen gerealiseerd worden, ook als de afmetingen van deze processen in de toekomst verder afnemen. Dit proefschrift onderzoekt daarom banddoorlaatfilters gebaseerd op deze N-path techniek, waarvan er verscheidene zijn ontworpen en gerealiseerd.

De maximale onderdrukking in traditionele N-path filters wordt beperkt door de weerstand van de schakelaars. In dit proefschrift wordt een 4^e orde banddoorlaat filter geïntroduceerd dat is gebaseerd op het verschil tussen twee 2^e orde filters met iets verschillende centrum-frequentie, mogelijk gemaakt door een G_m-C techniek. Dit filter elimineert het effect van de weerstand van de schakelaars op de maximale onderdrukking in de stopband. Het filter is gerealiseerd in 65 nm CMOS. De metingen laten zien dat dit filter een stopbandonderdrukking van meer dan 55 dB heeft, 40 dB meer dan conventionele N-path filters, en een betere vorm van de doorlaatband. IIP3 in de doorlaatband is +9 dBm, en in de stopband ($\Delta f = 50$ MHz) +29 dBm. De centrumfrequentie is instelbaar van 0.4 GHz tot 1.2 GHz.

Vervolgens wordt een ontwerpmethode voorgesteld voor de synthese van actieve N-path filters. Om deze methode te verifiëren is een 6^e orde 8-pad RF filter in 65 nm CMOS gerealiseerd. Dit filter haalt 59 dB stopbandonderdrukking, 25 dB versterking en een rimpel van < 0.6 dB in de doorlaatband. De versterking helpt om de eisen aan de ruis in de volgende trappen van de ontvanger te vergemakkelijken. Het filter dankt de goede vorm van de doorlaatband aan het gebruik van een Miller-compensatie methode. IIP3 in de doorlaatband is -12 dBm, en in de stopband ($\Delta f = 50$ MHz) $+26$ dBm. Het 1 dB compressiepunt voor interferentie op $\Delta f = 50$ MHz ligt op $+7$ dBm. Dit filter heeft een ruisgetal van 2.8 dB. Dit is bijna 7 dB lager dan dat van het vorige filter, voornamelijk te danken aan het feit dat de G_m cellen nu op RF frequenties werken en dus minder last hebben van $1/f$ ruis. De centrum-frequentie is instelbaar van 0.1 GHz tot 1.2 GHz en de bandbreedte is 8 MHz. Het filter bestaat uitsluitend uit inverters, schakelaars en capaciteiten en is dus goed schaalbaar naar kleinere CMOS technologieën.

Tenslotte wordt een techniek voorgesteld om de banddoorlaat-eigenschappen van een 6-pad filter op de 2e en 3e harmonische van de klokfrequentie te onderdrukken. Eén van de problemen van N-path filters is de herhaling van de banddoorlaat-karakteristiek op hogere harmonischen van de klokfrequentie. Interferentie op deze frequenties wordt met weinig verzwakking doorgelaten en vermindert de gevoeligheid van de ontvanger achter het filter. Simulaties in 28 nm FDSOI laten zien dat een 3^e harmonische onderdrukking van 40 dB mogelijk is. Ook wordt een methode geïntroduceerd waarmee het mogelijk is de overdracht van N-path filters over een groot frequentiebereik uit te rekenen op een aanzienlijk eenvoudiger manier dan tot dusver uit de literatuur bekend is. Met deze methode kan ook het effect van parasitaire capaciteiten op een intuïtieve en eenvoudige manier gevonden worden.

Abstract

Nowadays, wireless devices cover numerous wireless communication standards where almost for each one, a different frequency band has been allocated. There is a strong motivation towards SoC (System-on-Chip) solutions, where everything is integrated inside a chip to reduce the cost and form-factor of wireless devices. In radio-frequency receivers, due to the existence of large out-of-band blockers and a limited dynamic range, band-select filtering of the input signal is essential. Currently, most of the front-end circuitry of transceivers can be integrated on-chip. However, it is not possible to build integrated high-performance bandpass filters even after more than a decade research on this very topic. The inherent losses associated with on-chip inductors lead to filters having relatively high insertion losses, limited dynamic range and low out-of-band rejection. For this reason, nowadays, most wireless systems utilize individual off-chip filters rather than fully integrated bandpass filters. This increases the size and cost. Moreover, most current wireless devices have several standards which leads to the exploitation of numerous off-chip bandpass filters which further exacerbate the size and cost issues.

Although G_m-C and Q-enhanced LC RF bandpass filters are not capable to deliver high performance and wideband tunablitiy, N-path bandpass filters are. N-path filters are old and were forgotten. N-path filters can provide us with bandpass filters having high Q-factors and wide center-frequency tuning range. The center frequency of the N-path bandpass filter is set by its clock frequency and its bandwidth is determined by the value of its capacitors and source resistance. The principal constituents of N-path filters are switches, capacitors and a digital circuitry for providing clock signals needed for the operation of these filters. CMOS technology can offer very linear switches, high density capacitors and very fast digital gates. Therefore, CMOS technology is the best candidate for the implementation of N-path bandpass filters which are friendly with process scaling. Consequently, this thesis investigates the possibilities of RF bandpass filters with high selectivity, high dynamic range and wide center-frequency tuning range based on N-path filter technique. In this thesis, several bandpass filters based on N-path technique have been designed and implemented.

The ultimate rejection of classical N-path filters is limited due to a non-zero switch

resistance. A widely tunable 4th order bandpass filter based on the subtraction of two 2nd order 4-path filters having a second set of switches with slightly different center frequencies, generated by a G_m-C technique, is proposed. This filter eliminates the effect of switch resistance on the stopband rejection of the filter. As a proof of concept, this filter is implemented in CMOS LP 65 nm. Measurement results demonstrate that this filter achieves > 55 dB stopband rejection (40 dB better than conventional N-path filters) and better passband shape compared to conventional N-path filters. The in-band and out-of-band IIP3 of the filter are +9 dBm and +29 dBm ($\Delta f = 50$ MHz), respectively. The center frequency of the filter is tunable from 0.4 GHz to 1.2 GHz.

Afterwards, a design methodology for synthesis of general active N-path bandpass filters is proposed. To verify the theory, a tunable 6th order 8-path RF channel-select filter in CMOS LP 65 nm is introduced. The filter achieves a stopband rejection of +59 dB, passband gain of +25 dB and passband ripples < 0.6 dB. In this way, while the blockers are eliminated by filtering, the passband gain of the filter relaxes the noise requirement of the following stages in the receiver. The proposed filter achieves a good passband shape thanks to utilizing a Miller compensation method. The in-band and out-of-band IIP3 of the filter are −12 dBm and +26 dBm ($\Delta f = 50$ MHz), respectively. The filter is capable of obtaining 1dB blocker compression point of +7 dBm ($\Delta f = 50$ MHz). This filter has an average noise figure of 2.8 dB which is almost 7 dB better than our previous work. Compared to the previous proposed filter, this filter can achieve lower noise figure due to the exploitation of G_m cells in RF frequency instead of IF frequency. The center frequency of the filter is tunable from 0.1 GHz to 1.2 GHz and the bandwidth of the filter is 8 MHz. The proposed filter only consists of inverters, switches and capacitors and therefore it is friendly with process scaling. This filter defines the state-of-the-art of RF BPFs.

Finally, a technique to concurrently eliminate the bandpass shapes at second and third harmonics of clock frequency of a 6-path filter is proposed. One of the issues of N-path filters is the repetition of the bandpass shapes at higher harmonics of the clock frequency. Blockers located at these frequencies, that are passed with less attenuation, can degrade the sensitivity of a receiver that comes after the filter. Simulations in CMOS 28 nm FDSOI show the possibility of obtaining a third harmonic rejection of 40 dB. Moreover, a compact method to calculate the transfer function of N-path filters over a large frequency range is introduced which avoids the lengthy analysis presented in literature so far and also through a simple and intuitive method, the effect of parasitic capacitance on the performance of N-path filters is found.

Contents

Chapter 1

Introduction

1.1 Wireless Transceivers

Nowadays, wireless communication is an indispensable part of our life. Standards like GSM, WCDMA and EDGE are devoted to voice and data communications. Navigation has become equivalent to using GPS. Thanks to WLAN, a fast wireless Internet and peer-to-peer connections are available. Bluetooth empowers low power and short range connectivity between different devices. Near Field Communication (NFC) is an emerging standard that targets applications such as contactless transaction and data exchange. It is quite intriguing to have all the above mentioned services in a small cell-phone.[1] Mobile phone technology has come a long way since the first mobile phone call was made 40 years ago [2]. If we compare the first available mobile phone with a recent one, there is a huge difference between their size, cost, power consumption and functionality. This is mainly due to: 1) the scaling of VLSI processes, particularly CMOS technology, and 2) innovations in RF architectures, circuits and devices [3]. In fact, the minimum feature size of CMOS technology has fallen from 5 μm in 1972 [4] to 19 nm in 2013 [5].

The first mobile phone (Motorola DynaTAC) [2] was 23 cm tall, comprised 30 circuit boards, had a talk-time of 35 minutes, took 10 hours to recharge and had a price of $3,995$ \$. The first mobile phone and a modern one (Apple iphone 5) are illustrated in Fig. 1.1 for a comparison. To demonstrate the sophistication of current mobile phones, the circuit board of the latter is shown in Fig. 1.2. As can be seen, the two sides of the PCB have been fully filled in with numerous ICs from different manufacturers.

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[1]In contrast, Martin Cooper, the inventor of the first mobile phone, says: "They (cell-phones) all try to be universal. If you try to build a device that does all the things for all people, it will not do any of them very well. So i think that is where we are with cell-phones today"[1].

Figure 1.1: (a) The first mobile phone made by Motorola (DynaTAC) (b) The latest smart phone made by Apple (iphone 5).

1.2 Motivation

Almost each previously mentioned wireless standard occupies a different frequency band. Fig. 1.3 demonstrates the frequency bands allocated to different wireless standards. A generic multi-standard receiver and the block diagram of a typical receiver are illustrated in Fig. 1.4(a) and Fig. 1.4(b), respectively. As can be seen, copious amount of off-chip bandpass filters (BPF) are used. These BPFs are off-chip, bulky and expensive and hence increase the cost and form-factor. One approach to reduce the form-factor and size of wireless devices is to use SiP (System-in-Package) solutions where a BPF fabricated in a piezoelectric substrate and a CMOS transceiver chip are stacked together inside a package [7]. As an example, see parts 3, 4, 12 and 18 in Fig. 1.2. To further reduce the cost and form-factor of wireless devices, there is a strong motivation towards SoC (System-on-Chip) solutions, where everything is integrated inside a chip. Therefore, it is interesting to come up with solutions that eliminate the demand for off-chip BPFs. Two possible options are: 1) come up with novel circuits and receiver architectures that do not require these BPFs; and 2)

(1)Skyworks: GSM/GPRS/EDGE PA module
(2)SWUA: RF ant. switch module
(3)Triquint: WCDMA/HSUPA PA/duplexer module
(4)Avago: LTE PA+FBAR duplexer module
(5)Skyworks: CDMA PA module
(6)Avago: LTE band 13 PA

(7) Qualcomm: RF power management IC
(8) Hynix: 16 GB NAND flash
(9) Apple: power management IC
(10) Apple: Cirrus Logic Class D Amplifiers
(11) STMicroelectronics: Gyroscope
(12) Murata: Wi-Fi module

(13)STMicroelectronics: accelerometer
(14)Texas Instruments: touch screen SoC
(15)Broadcom: touchscreen controller

(16)Apple: processor
(17)Qualcomm: LTE modem
(18)Qualcomm: Multi-band/mode RF TRx

Figure 1.2: The circuit board of a modern smart phone (iphone 5) [6]: (a) The upper side of PCB (b) The lower side of PCB.

substitute these off-chip filters with integrated ones.

These off-chip BPFs considerably attenuate large undesired signals, located outside the band of interest, and hence ease the detection of desired signals. As an example, the in-band and out-of-band GSM receiver blocking level test is depicted in Fig. 1.5. This figure implies that the GSM receiver should cope with out-of-band blockers with $P_b = 0$ dBm while successfully detecting a desired signal with power level of -98 dBm. Without filtering, this 98 dB of difference, is quite difficult to handle.[2] Therefore, the first option seems to be rather impractical.

The second option is to substitute off-chip BPFs with integrated ones. In this thesis, we will focus on exploring methods for designing integrated RF BPFs with large out-of-band signal-handling capabilities without sacrificing the sensitivity of the

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[2]A typical off-chip BPF for GSM band can be found in [8]. Usually, the amount of required rejection is found by the fact that the effective strength of undesired out-of-band signals should be at most equal to the largest in-band interferer. For example, in GSM standard, the pre-filter should provide at least 23 dB of rejection for 0 dBm undesired signals.

Figure 1.3: Frequency band allocations of different wireless standards used in mobile phones.
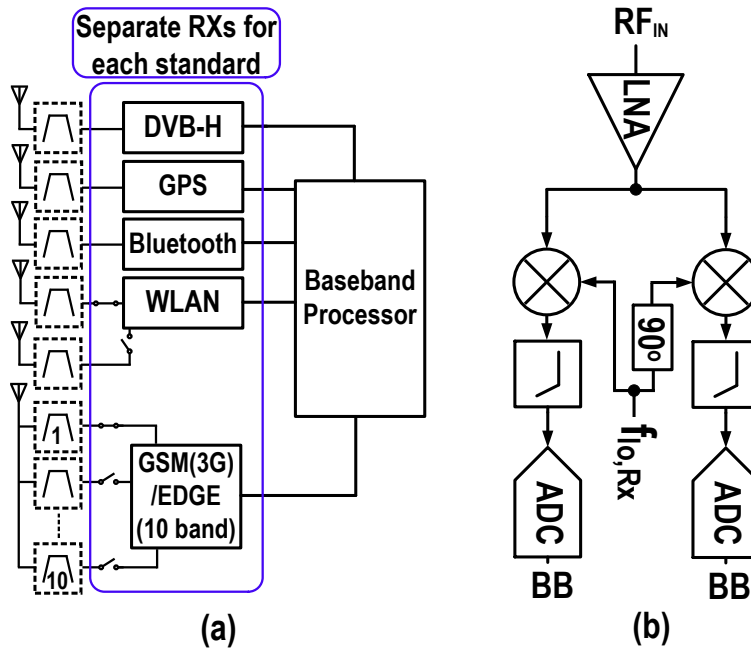
Figure 1.4: (a) A generic multi-standard receiver where each standard has a separate receiver (b) A block diagram of typical receivers used in (a).
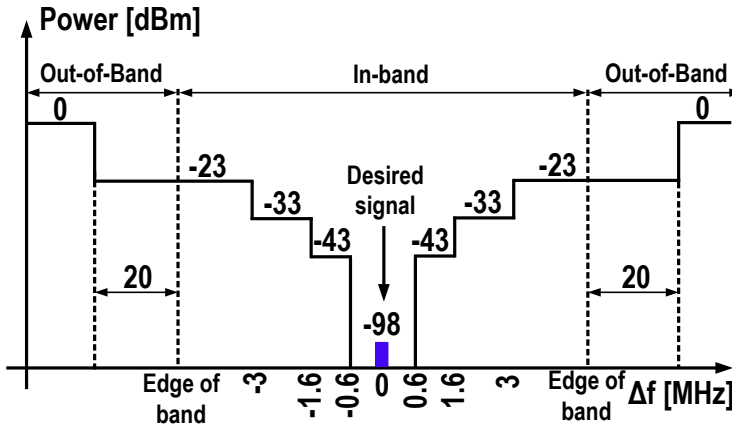
Figure 1.5: GSM receiver blocking test [3]. (The desired channel center frequency is denoted by 0 for simplicity).

receiver that comes after it. Also, these filters should have high selectivity, and wide center-frequency tuning range to cover different frequency-bands and save area.
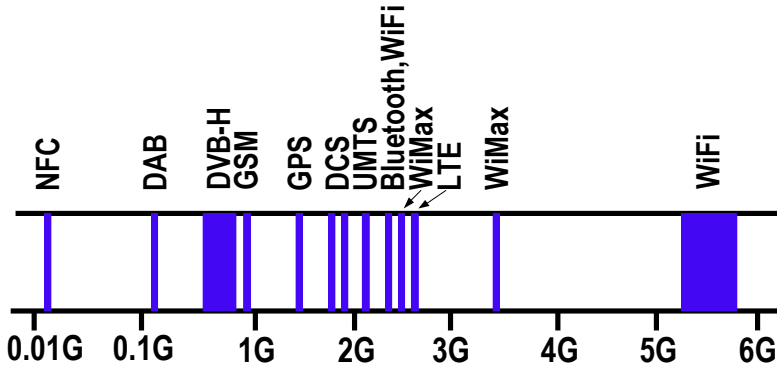
1.3 Thesis Outline

In *chapter 2*, a summary of different approaches to the integration of RF BPFs will be given. Issues such as frequency response stability, high-frequency performance, signal-handling capability, noise and power dissipation will be addressed for each approach. Accordingly, the choice for N-path filters will be motivated.

In *chapter 3,4* and *5*, several BPFs are designed based on the N-path filter technique. In *chapter 3*, a widely tunable 4th order BPF based on the subtraction of two 2nd order 4-path filters with slightly different center frequencies, generated by a G_m-C technique, is proposed. This filter achieves larger stopband rejection and better passband shape compared to conventional N-path filters.

In *chapter 4*, a widely-tunable and highly-selective filter with a decent amount of embedded amplification is introduced. In this way, while the blockers are eliminated by filtering, the passband gain of the filter relaxes the noise requirement of the following stages in the receiver. Furthermore, the design methodology for synthesis of active N-path BPF is introduced. Based on this methodology, a tunable 6th order 8-path RF channel-select filter is introduced. It is based on coupling N-path filters with gyrators, achieving a "flat" passband shape and high out-of-band linearity. A technique is utilized to considerably improve the passband shape of the filter. The proposed filter only consists of inverters, switches and capacitors and therefore it is

friendly with process scaling. Compared to the filter technique introduced in *chapter 3*, this filter can achieve lower noise figure due to the exploitation of G_m cells in RF frequency instead of IF frequency.

In *chapter 5*, a technique to concurrently eliminate the bandpass shapes at second and third harmonics of a 6-path filter is proposed. In conventional N-path filters, blockers located at the second and third harmonics of the clock frequency are passed which can degrade the sensitivity of a receiver that comes after the filter. Moreover, a compact method to calculate the transfer function of N-path filters over a large frequency range is introduced which avoids the lengthy analysis presented in literature so far and through a simple and intuitive method, the effect of parasitic capacitance on the performance of N-path filters is found.

In *chapter 6*, conclusions and an overall summary of the thesis will be given. Moreover, the original contributions will be pointed out and some directions for future research will be proposed.

Chapter 2

Approaches to Integrated Analog Bandpass Filters

2.1 Introduction

Wireless communication systems continue to evolve, supporting multiple standards while facilitating a growing number of portable wireless devices operating in a common frequency spectrum. The success of commercial wireless communication products is due, in part, to the inclusion of highly integrated radio frequency (RF) transceivers which feature low cost, low power consumption, and performance levels that meet demanding system specifications. The architecture of integrated RF transceivers has been largely determined by RF bandpass filter performance and system requirements [9]. Early radio architectures such as super-heterodyne needed several bandpass filters (BPF) in the receiver or transmitter chain to suppress interference and image signals. These filters were typically off-chip, bulky and expensive which led to penalties in terms of cost, form factor and less design flexibility. The push towards single-chip solutions led to a tremendous amount of research on the integration of these bandpass filters [9, 10, 11, 12, 13, 14, 15, 16]. Analog BPFs have been notoriously difficult to implement on-chip. Due to the lack of success in implementation of RF BPFs having both high DR and high Q-factor, designers explored other possible architectural solutions such as zero- or low-IF receivers where the amount of required bandpass filtering is much lower compared to conventional heterodyne receivers [17]. These types of receivers have to cope with other issues such as $1/f$ noise, LO self-mixing, DC offsets and etc. [3]. However, these issues have been alleviated through extensive digital calibrations [3]. One remaining issue that has not been resolved is the fundamental limitation on the DR of the direct-conversion receivers. By moving all the channel-

select filtering to the baseband sections, the low-noise amplifier (LNA) which should have sufficient gain is subjected to the full RF spectrum. Thus, strong out-of-band and out-of-channel blockers can severely desensitize the receiver. Therefore some pre-select filtering is required before the LNA which nowadays is typically done using off-chip BPFs such as surface acoustic wave (SAW) filters. The possibility of improving the DR of the receiver by removing the LNA and the BPF from the receiver chain has been proposed in [18, 19]. However, these type of receivers (mixer-first receiver) are quite power hungry for achieving the desired sensitivity and this issue exacerbates with down-scaling of the technology. Thus, the need for high-frequency, high-Q BPFs can not be eliminated. In this chapter, a summary of different approaches to the design of integrated BPFs will be given. Moreover, issues such as *frequency response stability*, *high-frequency performance*, *signal-handling capability*, *noise* and *power dissipation* will be addressed for each approach.

2.2 Q-enhanced LC BPF

Integrated RF filters based on LC topologies exhibit poor performance because on-chip inductors have low quality factors. The effects of the limited Q-factor of on-chip inductors in multi-pole BPFs are namely a significant drop in the insertion loss of the filter and a considerable reduction in the shape-factor of the filter ("shoulder droop") [20]. Obtaining a near ideal bandpass response requires inductors with quality factors of approaching 200 or more [21]. In fact, for the same bandwidth, as the order of the filter increases, the minimum tolerable Q-factor of inductors increases very rapidly [20]. The best available monolithic inductor in silicon substrate achieves Q-factors in the range of $10-30$ depending on inductance value and frequency [21]. Clearly, some form of enhancement is required to make viable integrated RF LC BPFs.

2.2.1   Operation

The two most popular topologies that have been utilized in integrated BPF design are series-C coupled resonators and shunt-C coupled resonators as illustrated in Fig. 2.1 [22]. These BPFs have the least spreads in their component values and moreover use a low number of inductors [22]. Conventionally a negative resistance is exploited to cancel the losses associated with monolithic inductors. As can be seen in Fig. 2.1, the negative resistance can be located in series or in parallel with the inductor. The location and the type of the negative resistance have a great impact on the passband distortion of Q-enhanced BPFs [16, 20, 21, 23, 24]. A very first-order model of an on-chip inductor where only the series ohmic loss is taken into account is shown in Fig. 2.2. Using narrowband approximations, a series RL can be converted to a parallel one [25] as depicted in Fig. 2.2. As can be seen, the parallel resistance, R_p, is a strong
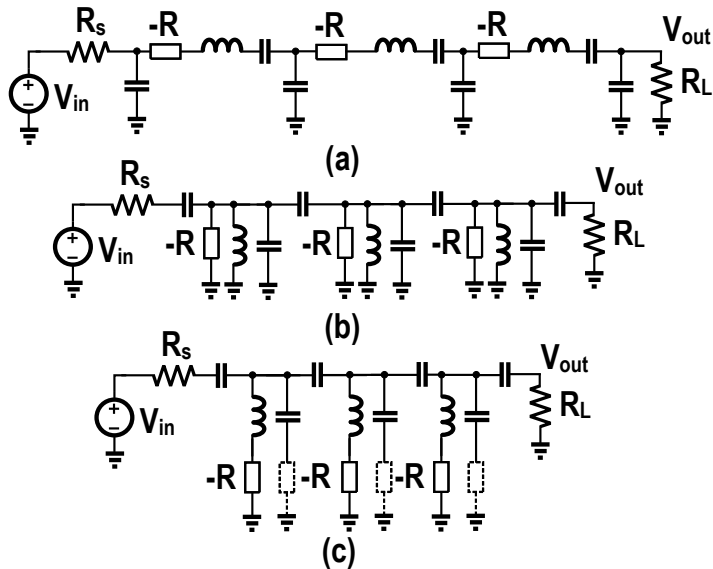
Figure 2.1: (a) Shunt-C coupled resonator BPF using series negative resistance to cancel the loss of inductors (b) Series-C coupled resonator BPF utilizing parallel negative resistance (c) Series-C coupled resonator BPF utilizing series negative resistance with either inductor or capacitor.

function of frequency. Here, we should make a critical observation. If a series negative resistance is used, it should not have frequency dependency and if a parallel one is exploited, it should have the same dependency on frequency as R_p does. Deviation from these rules will lead to a distortion in the passband shape of the filter [23]. Different types of negative resistors that have been used in *Q*-enhanced LC BPFs are shown in Fig. 2.3.

2.2.2 Performance

While many definitions of DR exist, a simple and useful one in comparing different circuits is:

$$\mathrm{DR} = \frac{\mathrm{P_{1dB}}}{\mathrm{P}_n} \tag{2.1}$$

where $\mathrm{P_{1dB}}$ is the 1-dB output compression power and P_n is the output noise floor [14]. It can be shown that the DR of a 2$^{\mathrm{nd}}$ order *Q*-enhanced LC BPF shown in Fig. 2.4 is:
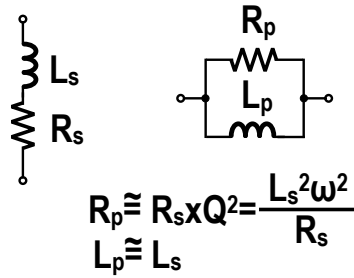
Figure 2.2: A first-order model of an on-chip inductor where the series ohmic loss is taken into account and its parallel counterpart.
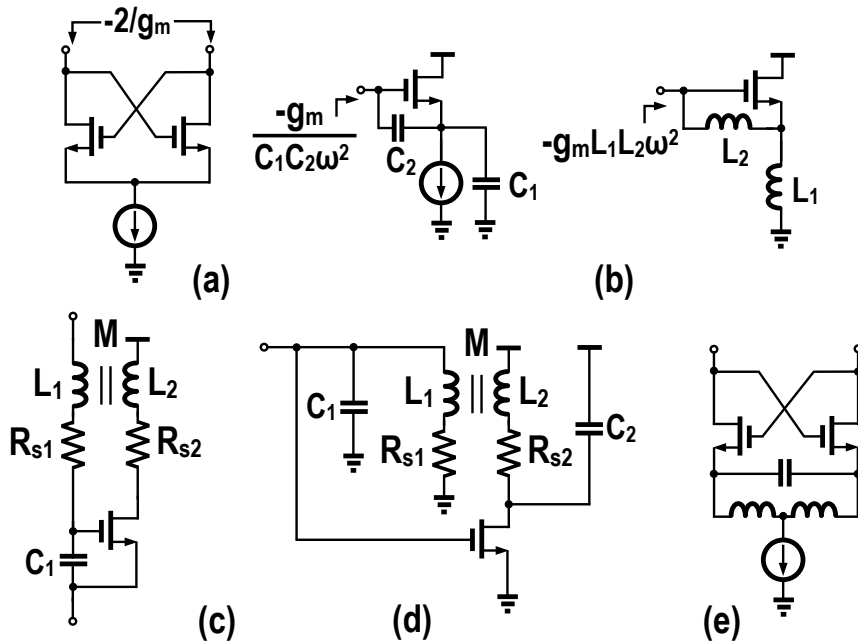
Figure 2.3: Different types of negative resistors: (a) A constant and differential one (b) Frequency dependent negative resistors [16] (c) A series LC tank with a constant series negative resistance [20] (d) A parallel LC tank with a constant negative resistance in series with its inductor [21] (e) A modified differential negative resistance [21, 24].
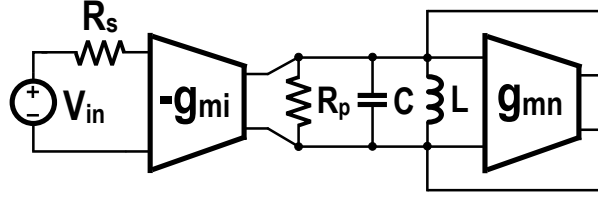
Figure 2.4: A typical 2$^{\text{nd}}$ order *Q*-enhanced LC BPF

$$\text{DR}_{\text{QELC}} = \frac{\eta \text{P}_{\text{DC}}}{4k\text{T}(1+\gamma)\text{B}} \times \left(\frac{Q_0}{Q}\right)^2 \tag{2.2}$$

Where η is the efficiency of the circuit, B is the bandwidth of the filter, γ is the noise excess factor of the G_{m} cells, Q_0 is the uncompensated *Q*-factor of the inductor and Q is the *Q*-factor of the filter [14]. (2.2) tells us that increasing the raw quality factor of on-chip inductors has a great impact on the dynamic range of *Q*-enhancement filters [26, 27]. The DR of an LNA can be described by:

$$\text{DR}_{\text{LNA}} = \frac{\eta \text{P}_{\text{DC}}}{k\text{TFGB}} \tag{2.3}$$

where F is the noise factor, B is the bandwidth and G is the power gain of the LNA. By comparing (2.2) and (2.3), it can be deduced that to achieve a DR similar or better than an LNA, we should have:

$$Q_0 \geq 2Q\sqrt{\frac{1+\gamma}{\text{FG}}} \tag{2.4}$$

For example[1], if F = 2 dB and G = 18 dB, Q/Q_0 of up to 3 is theoretically permissible [14]. The linearity and the noise performance of the filter is limited by the negative resistance. In fact, the addition of the negative resistance: 1) modifies the P_{1dB} of the circuit to $\text{P}_{\text{1dB}}Q_0/Q$ and 2) modifies the P_{n} of the circuit to $\text{P}_{n}Q/Q_0$. Although there has been more than a decade research on these types of BPFs, most of the designs do not achieve enough DR which is to a first degree is due to the limited *Q*-factor of on-chip inductors [9, 10, 11, 12, 13, 14, 15, 16, 20, 21, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33].

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[1]Values in (2.4) are not in dB.
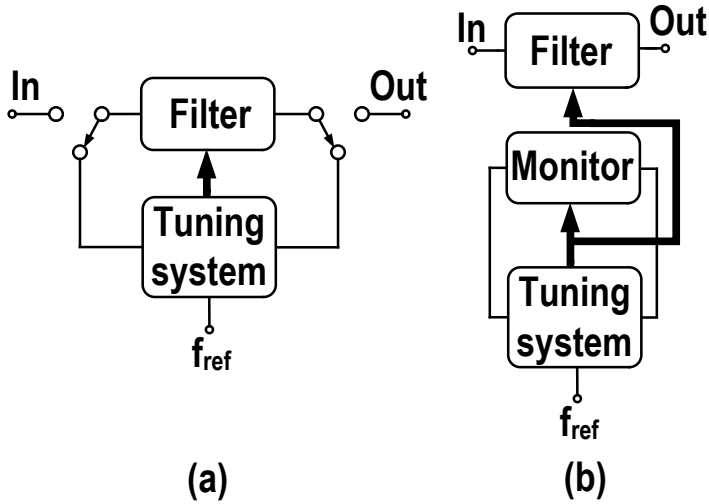
Figure 2.5: Automatic tuning: (a) Direct (b) Indirect.

2.2.3 Frequency Response Stability

In general, fabrication tolerances and temperature variations can modify the transfer function of the filter due to the change in the value of its components. In fact, the sensitivity of the filter transfer function to component values increases as the Q-factor increases. Therefore, to have a stable transfer function over PVT variations, some sort of correction circuitry is required. Two general methods are illustrated in Fig. 2.5 [34, 35]. A filter is placed in a feedback loop and its frequency response is adjusted until it becomes locked to an off-chip stable reference such as a clock frequency, f_{ref}, as shown in Fig. 2.5(a). If the filtering function cannot be interrupted periodically, two identically constructed on-chip filters may be used in time-interleaved fashion between tuning and system operation [34, 35]. As an alternative approach, a replica of a basic block of the filter is automatically tuned continuously, and the control signal used for that is also applied to the main filter, as shown in Fig. 2.5(b) [34, 35]. This is known as "Master-Slave"technique. Good matching between the filter and the monitor block is an essential requirement for this method. Usually, two parameters of the filter, namely the center frequency and the Q-factor should be corrected in BPFs. A popular method for tuning the Q-factor and the center frequency of the Q-enhanced LC filters is shown in Fig. 2.6 [9, 16, 23, 34, 35]. As can be seen, it is based on an indirect automatic tuning of the filter (Fig. 2.5(b)) and consists of two loops, one for frequency tuning and one for Q-factor tuning.

In summary, current Q-enhanced LC BPF are not suited for RF front-ends applica-
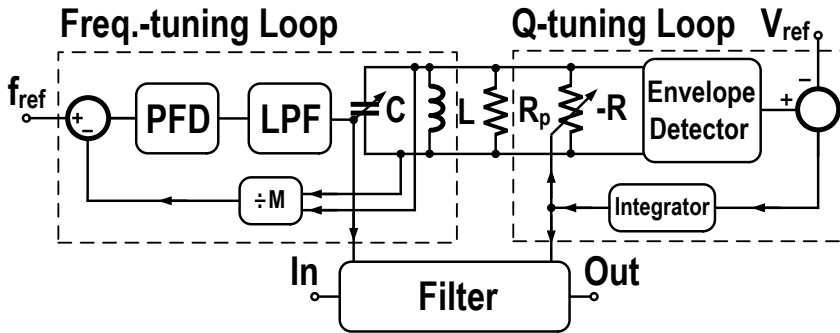
Figure 2.6: A conventional method for tuning the Q-factor and the center frequency of the Q-enhanced LC filters.

tions. However, they can be exploited in the transmitter chain after the up-conversion mixer where the required DR is not demanding [36]. Also in [37], a high-order LC BPF by exploiting high Q-factor bond wires has been implemented which have more than 10 dB of insertion loss. An extensive comparison table is given in [24].

2.3 G_m-C BPFs

G_m-C BPFs exhibit inferior performance (e.g., lower DR) compared to the Q-enhanced LC BPFs. This is mainly caused by the fact that in G_m-C BPFs, an additional active circuitry is needed to synthesize inductors. This leads to more power consumption and less DR compared to Q-enhanced LC BPFs. Moreover, the excess phase-shift of the G_m cells utilized in these filters, greatly impacts the passband shape and the stability of this type of BPFs.

2.3.1 Operation

The integrator is the main building block of G_m-C BPFs which is implemented by a transconductance element loaded with a capacitor. All the state equations of the desired LC BPF prototype can be found and a G_m-C based integrator can be utilized to synthesize the filter [34, 35]. Another approach which is much easier than the first approach is the utilization of gyrators. It is known that an inductor can be synthesized by a gyrator loaded with a capacitor. Therefore, to design a G_m-C BPF, we start with a desired LC BPF prototype and substitute all the inductors with its gyrator-based counterpart [35, 38, 39]. The quality of these active inductors determines the attainable maximum center frequency, Q-factor and the DR of this type of filters. Fig. 2.7(a) shows the synthesis of an inductor by a gyrator loaded with a capacitor.
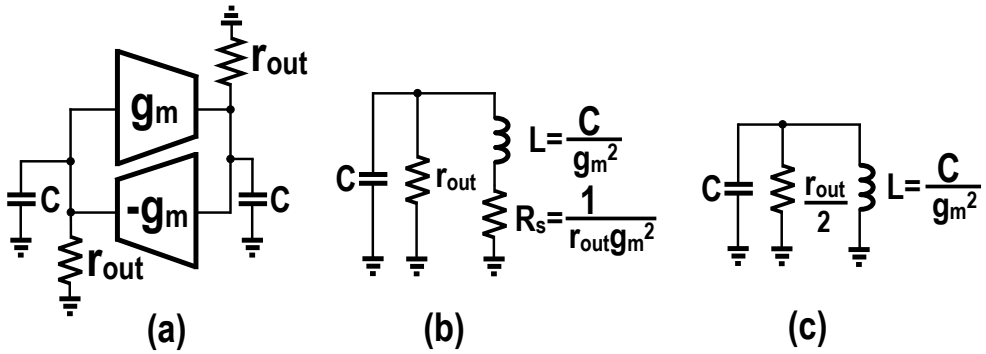
Figure 2.7: (a) An LC resonator where the inductor is synthesized using a gyrator (b) Modeling the active inductor by a lossy passive inductor (c) Its narrow-band approximation.
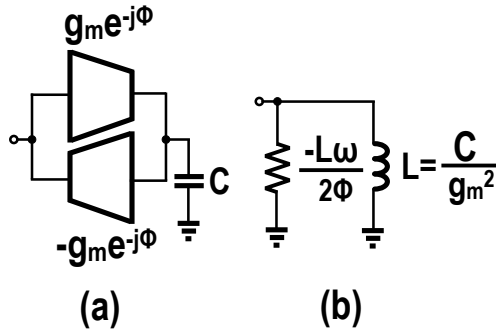
Figure 2.8: Modeling the extra phase-shift of the G_m cells by a parallel negative resistance.

The gyrator is realized by two G_m cells having a finite output resistance of r_{out} connected in a negative feedback. The active inductor can be modeled by a lossy inductor as shown in Fig. 2.7(b). This circuit can be further simplified using narrow-band approximations [25] as illustrated in Fig. 2.7(c). Because the value of active inductor is C/g_m^2, the center frequency of the filter is g_m/C. The Q-factor of the filter is therefore $Q = 0.5g_m r_{out}$, where $g_m r_{out}$ is the DC gain of the G_m cells. In other words, the limited DC gain of the G_m cells puts a fundamental limit on the achievable Q-factor of G_m-C BPFs. It is possible to increase the output resistance of the G_m cells by cascoding [38]. However, this leads to an additional phase-shift due to internal non-dominant poles of the G_m cells. It can be shown that these extra phase-
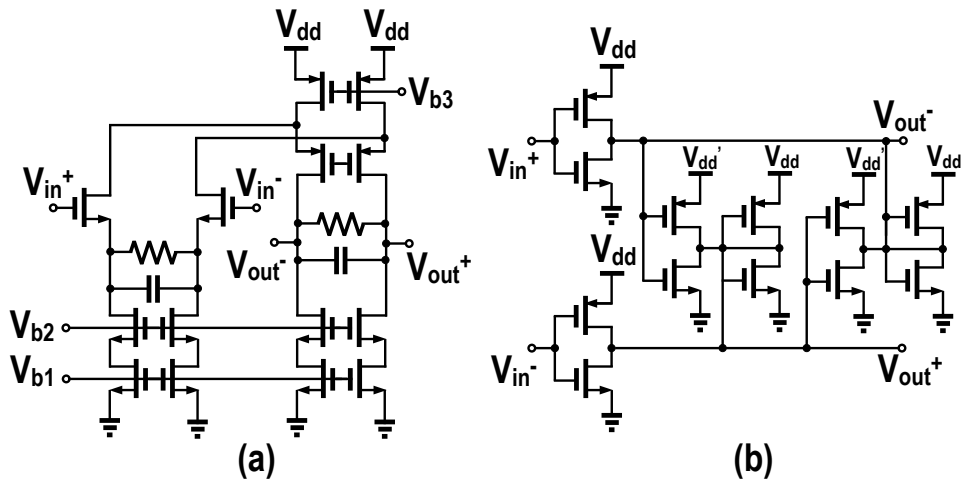
Figure 2.9: High DC gain G$_m$ cell: (a) by cascoding which introduces extra non-dominant poles [40] (b) by using negative resistance which does not introduce any extra phase-shift [39].

shifts lead to an additional negative resistance in parallel with the active inductor [38] as illustrated in Fig. 2.8. This effect can be exploited to compensate the loss of the active inductor due to the finite output resistance of the G$_m$ cells. However, the exact modeling of the extra phase-shift due to non-dominant poles is a difficult task. In contrary, an elegant approach to improve the DC gain of the G$_m$ cells has been proposed in [39] where explicit negative resistors are exploited to increase the DC gain of G$_m$ cells without the addition of any undesired poles (Fig. 2.9(b)).

2.3.2 Performance

It can be shown that the DR of a 2nd order G$_m$-C BPF shown in Fig. 2.10 is described by [14]:

$$\text{DR}_{\text{GMC}} = \frac{\eta \text{P}_{\text{DC}}}{8k\text{T}(1+\gamma)\text{B}Q^2}. \tag{2.5}$$

In the resonance frequency, the current through the capacitor, I$_c$, is Q times larger than the current drawn by the parallel resistance, I$_{in}$ [25]. I$_c$ should be supplied by the G$_m$ cells making the gyrator. Therefore, the 1-dB output compression power P$_{1dB}$ of the filter is limited by the G$_m$ cells making the gyrator. In this way, P$_{1dB}$ is Q times lower than the case where a passive inductor is utilized. Moreover, it can be shown that the output noise power of the filter is 2Q times larger compared

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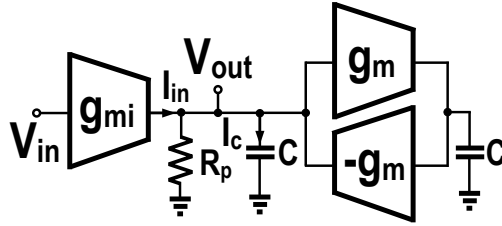
Figure 2.10: A 2nd order G$_m$-C BPF.
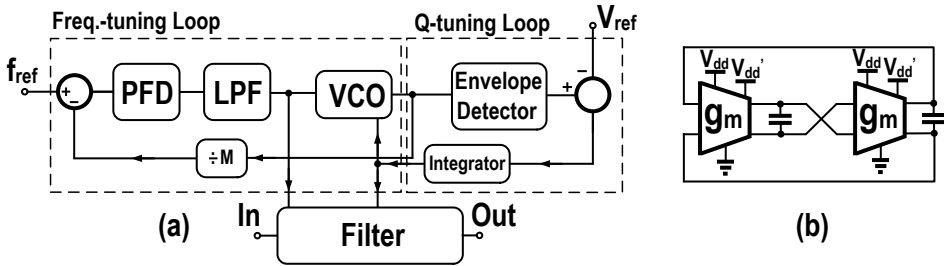
Figure 2.11: (a) Combined frequency- and Q-tuning loops [39] (b) Voltage-controlled oscillator for the frequency- and Q-tuning circuit.

to the case of a utilized passive inductor [41]. Interestingly, comparing the dynamic range of G$_m$-C BPFs with Q-enhanced BPFs shows that G$_m$-C BPFs are Q_0^2 times inferior to Q-enhanced BPFs where Q_0 is the Q-factor of on-chip inductors. Due to this fundamental superiority of Q-enhanced BPFs over G$_m$-C BPFs, logically, all the published GHz range integrated active BPFs are based on Q-enhanced LC filters.

It is possible to mitigate the effect of Q-factor on the output noise of the filter simply by increasing the size of the capacitors by Q. To achieve the same center frequency as before, all the G$_m$ cells should be scaled up Q times ($\omega_0 = g_m/C$). This directly translates to Q times increase in the power consumption of the filter. Also as the center frequency, ω_0, of the filter increases, the required value of the G$_m$ cells should be increased proportionally ($g_m \propto \omega_0 Q$). As a consequence, the current consumption of the filter is directly proportional to the product of the center frequency,ω_0, and the Q-factor of the filter.

2.3.3 Frequency Response Stability

The sensitivity of G$_m$-C BPFs to process variations is higher than Q-enhanced LC BPFs. In general, two explicit feedback loops are required to correct the center
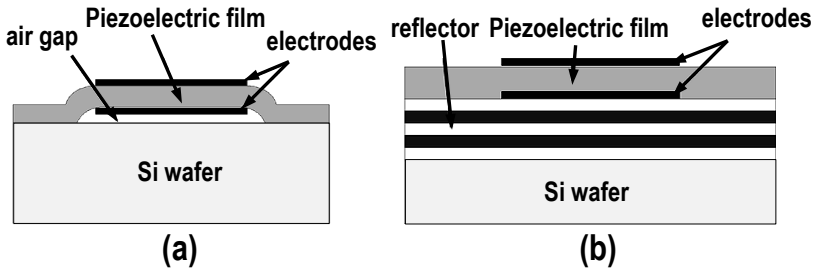
Figure 2.12: Configurations of BAW resonators: (a) Surface micro-machined FBAR (film bulk acoustic resonator) (b) SMR (solidly mounted resonator).
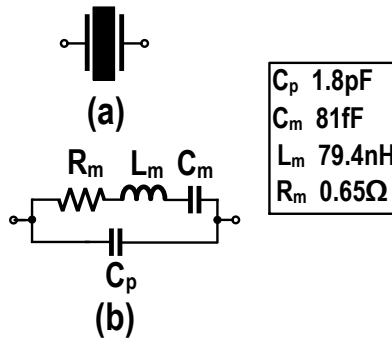
Figure 2.13: (a) A symbol of a resonator (b) An RLC modeling of a resonator; component values for a FBAR resonator also are given [43].

frequency and Q-factor of the filter [39, 42]. The frequency and Q-factor control loops that have been used in [39] are shown in Fig. 2.11.[2]

2.4 Micro-Mechanical Filters

One approach to the miniaturization of transceivers is to explore the possibility of integration of passive high-Q resonators. There are two distinct directions in this approach. The first one is the exploitation of CMOS compatible piezoelectric materials such as AlN. The second direction is the utilization of capacitive-transduction MEMS structures which are quite friendly with CMOS processing and provide us with very high Q-factors even in the air. In this section, we will give a summary of both directions.

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[2]In reality, the amplitude detector and control loop were built inside the VCO to prevent a possible instability due to the interaction of the Q-factor and f_c loops.
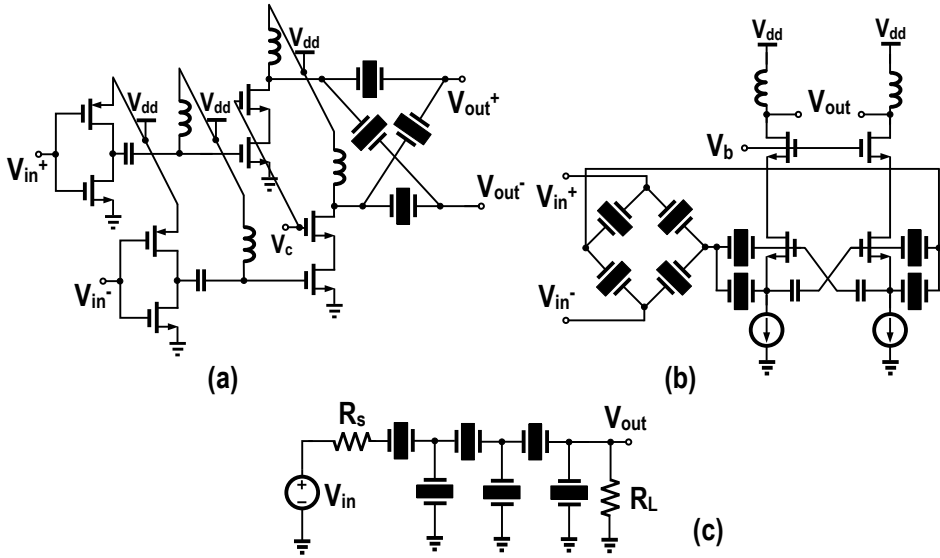
Figure 2.14: (a) Using a lattice filter in PA to filter out undesired signals [52] (b) Utilizing a double lattice configuration before LNA [50, 53] (c) Ladder BPF based on FBAR resonators [54].

2.4.1 Piezoelectric Resonators

The basic configuration of a BAW (Bulk Acoustic Wave) resonator is a piezoelectric thin film surrounded by two metal electrodes [43, 44, 45, 46, 47, 48, 49, 50, 51, 52]. Fig. 2.12 shows the two main configurations for realizing BAW resonators. The first resonator, also known as a film bulk acoustic resonator (FBAR), is a membrane structure suspended in the air by its edges. The second configuration is the solidly mounted resonator (SMR), in which the acoustic impedance of the substrate is transformed to a very low value to reduce the energy loss through the substrate and hence sustaining the high Q-factor of the resonator. In comparison with surface acoustic wave (SAW) devices, BAW resonators and filters exhibit a lower frequency drift with temperature [50]. The FBAR resonator can be modeled electrically as a series RLC circuit in parallel with a capacitor. This model is shown in Fig. 2.13 [43]. FBAR resonators can offer Q-factors in the range of 1k [43, 44, 45, 46, 47, 48, 49, 50, 52, 53]. In [43], a duplexer based on FBAR resonators was fabricated working at 1900 MHz (the PCS band), which was 10 times smaller than its off-chip counterpart and it was better than a SAW duplexer in terms of power handling [46, 47, 48].

In general, utilization of high-Q resonators leads to a considerable reduction in the power consumption of the receivers[55, 56, 57]. FBAR resonators are extensively

used in oscillator design leading to very low power and low phase-noise LO generations [43, 44, 45, 49, 53, 56, 58, 59]. In most cases, the FBAR resonators are wire bonded to the transistor chip. However, in [44], the resonator is directly integrated above the IC which leads to the reduction in the area. One of the issues of oscillators exploiting high-Q resonators is the limited tunability of this type of resonators which is mainly due to the inherent parallel capacitance of the resonators. In [45], a technique has been proposed to cancel this parallel capacitance. Here, some examples where the FBAR resonators have been utilized to design high-order BPFs will be discussed. In [52], A high-Q BAW lattice BPF was co-designed with a power amplifier as shown in Fig. 2.14(a). In [50, 53], a double lattice BPF before the LNA was exploited to relax the linearity requirement of the LNA and reduce its power consumption. The exploited double lattice configuration is shown in Fig. 2.14(b). Also, a ladder filter [22] based on FBAR resonators is shown in Fig. 2.14(c) [54]. BPFs based on FBAR resonators are the best options from DR and power consumption points of view. However, there are some issues associated with them that need to be addressed. One is the accuracy of the resonance frequency of the FBAR resonators. The resonance frequency of the FBAR resonators is inversely proportional to the thickness of the piezoelectric material. Although the lateral dimensions can be made quite accurate in the fabrication process (it is limited by the lithography.), the thickness of the layers are not very well controlled. This can potentially lead to a deviation in the center frequency of the resonators and filters [53]. Another issue is that they are not tunable. Therefore, to cover different frequency bands, a large arrays of them would be necessary that definitely increases the area and cost.

2.4.2 Capacitive-Transduction Resonators

There has been tremendous research on capacitive-transduction resonators due to their high compatibility with CMOS fabrication processes and their simplicity [60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76]. This has led to a large number of different structures for this type of resonators. In [62], it is proposed to exploit the mechanical nonlinearity of the resonator to achieve a Mixer-Filter ("Mixler"). Moreover, in [77], an interesting idea of resonant-gate transistor has been proposed which operates as a frequency-selective transistor.

Now, a brief explanation of how this type of resonators are operating, will be given. A simplified clamped-clamped beam resonator which is stimulated by an input voltage of $V_{DC} + V_{ac}$ is illustrated in Fig. 2.15(a) where $V_{ac} \ll V_{DC}$.[3] Using its simplified lumped spring-mass model shown in Fig. 2.15(b), its input impedance can be calculated [61]. The input impedance of the resonator consists of two parts, a

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[3]In other words, V_{DC} sets the mechanical DC point and V_{ac} acts like a small-signal perturbation around that point (similar to what we do in small signal analysis of transistors).
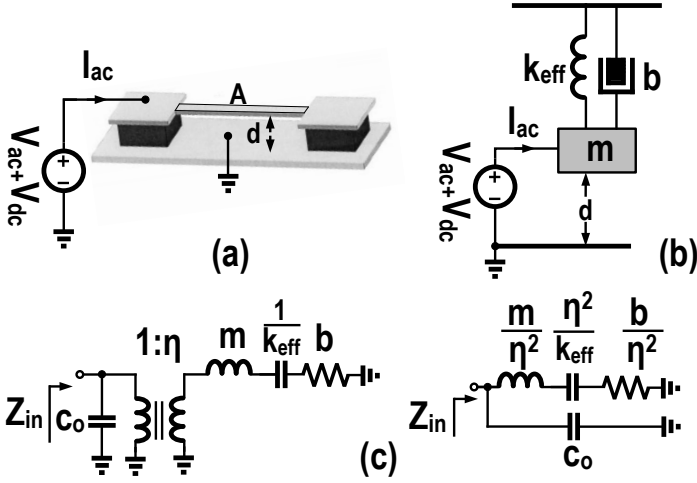
Figure 2.15: (a) A clamped-clamped beam resonator (b) A simplified lumped model of the resonator (mass-spring) (c) Equivalent input impedance of the resonator; η is the electrical to mechanical transduction.

series RLC tank and a parallel capacitance as illustrated in Fig. 2.15(c). The input impedance of the filter is:

$$Z_{in}(s) = \left(L_m s + \frac{1}{C_m s} + R_m \right) || \frac{1}{C_o s}$$

$$L_m = \frac{m}{\eta^2}, C_m = \frac{\eta^2}{k_{eff}}, R_m = \frac{b}{\eta^2}, C_m = \frac{\epsilon A}{d} \tag{2.6}$$

where A is the area of the resonator, d is the distance between the two plates of the resonator, ϵ is the permeability of the dielectric between the two plates, k_{eff} is the effective stiffness of the resonator, m is its mass, b is the damping factor of the resonator, and η is the electrical-to-mechanical transduction of the resonator which is approximately $\epsilon A V_{DC}/d^2$. The series resonance frequency and Q-factor of the resonator can be found by:

$$\omega_o = \sqrt{\frac{k_{eff}}{m}}$$

$$Q = \frac{\sqrt{m k_{eff}}}{b} \tag{2.7}$$

It can be shown that the stiffness of the resonator is not constant and it has a nonlinear relationship with the applied DC voltage, V_{DC}, as described by:
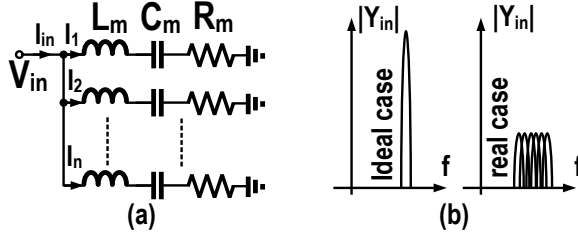
Figure 2.16: (a) Lowering the impedance level of the resonator by exploiting a large number of them in parallel (b) In ideal case, by paralleling n resonators, the input admittance of the resonator increases by n times; however, in reality due to the mismatch, this is not the case.

$$k_{\text{eff}} = k - \frac{\epsilon A V_{\text{DC}}^2}{2(d - x_0)^3} \tag{2.8}$$

where x_0 is the DC displacement point of the resonator. Interestingly, as V_{DC} increases, the effective stiffness of the resonator, k_{eff}, decreases. It is possible to exploit this property to tune the center frequency of the resonators. The tuning range is severely limited and practical achieved results show a tuning range of $\ll 1\%$. There is a specific input DC voltage ($V_{\text{pull-in}}$) and a DC displacement point ($x_{\text{pull-in}}$) (2.9) where k_{eff} will be zero and consequently the two plates of the resonator will stick to each other [61]. The dependence of the effective stiffness, k_{eff}, to the applied voltage (2.8) is the source of nonlinearity in the capacitive-transduction resonators leading to a worse linearity performance compared to SAW filters [68].

$$
\begin{aligned}
x_{\text{pull-in}} &= \frac{d}{3} \\
V_{\text{pull-in}} &= \sqrt{\frac{8d^3 k}{27 \epsilon A}}
\end{aligned}
\tag{2.9}
$$

One of the main issues of the capacitive-transduction resonators is their very large impedance level (e.g., 791 kΩ at $f_{\text{res}} = 1.5$ GHz) compared to resonators based on piezoelectric materials (e.g., 0.65 Ω at $f_{\text{res}} = 2$ GHz) [60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76]. One way to reduce the impedance level of these resonators is to exploit a large number of them in parallel as shown in Fig. 2.16(a). However, there is a big challenge in this approach. Due to the variations in the fabrication process and the high Q-factor of the resonators, it is quite difficult to add all the signals from all the paths in a constructive way as illustrated in Fig. 2.16(b). Alternatively, as can be seen from (2.6), increasing $\eta = \epsilon A V_{\text{DC}} / d^2$ will reduce
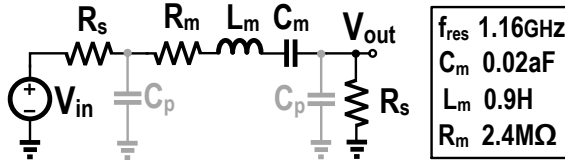
Figure 2.17: A 2nd order BPF based on a MEMS resonator where the equivalent RLC values of a MEMS resonator [64] are given as an example.

the input impedance of the filter. There are different possibilities: 1) increasing the area of the resonator, A; 2) reducing the gap distance, d; 3) Using dielectric materials with high permeability, ϵ; and 4) increasing the DC bias voltage of the resonator, V_{DC}. Reducing the gap distance, d, has the most significant impact on lowering the input impedance of the resonator, $R_m \propto 1/d^4$. According to [68], all of these options lead to a degradation in the linearity performance of the resonator.[4] Therefore, fundamentally, capacitive-transduction MEMS resonators suffer from a trade-off between their impedance-level and linearity.

The different types of capacitive-transduction resonators with a summary of their structures, frequency range, Q-factors, and motional resistances, R_m, are illustrated in Table 2.1. As can be seen, very high Q-factors even in the air is possible in GHz range frequencies. The motional impedance of the MHz range MEMS resonators is in range of $8 - 40$ kΩ. Currently, high-performance low-frequency oscillators based on MEMS resonators are commercially available [80]. However, the motional impedance of GHz range MEMS resonators is in MΩ range. A 2nd order BPF based on a MEMS resonator is illustrated in Fig. 2.17 where the equivalent RLC values of a MEMS resonator [64] are given as an example. It can be shown that the S_{21} of the filter is:
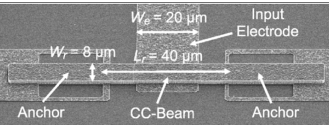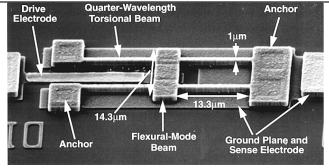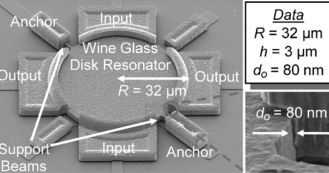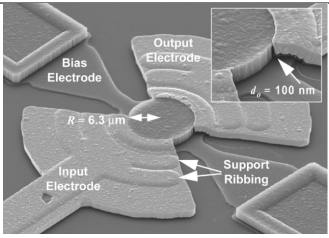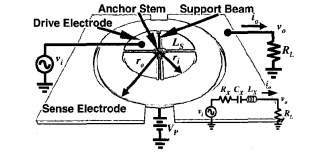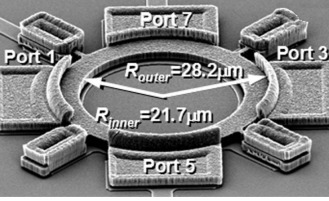
$$S_{21} = \left(1 + \frac{R_m}{2R_s}\right)^{-2} \tag{2.10}$$

which can be simplified to $(2R_s/R_m)^2$ for $R_m \gg R_s$. Therefore, high motional impedance, R_m, can lead to a notoriously low S_{21} (e.g., -80 dB in a 50 Ω environment [64]). According to (2.10), for a constant R_m, it is possible to increase S_{21} by increasing the value of the source and load resistance, R_s. However, the amount of improvement is limited at high frequency due to the presence of parasitic capacitors, C_p, as shown in Fig. 2.17.

In summary, currently low-frequency MEMS resonators are quite suitable for low-noise oscillator design having smaller form-factors compared to crystal oscillators [80].

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[4]This also can be seen by the fact that all the mentioned techniques lead to a reduction in the $V_{pull-in}$ of the resonator (2.9) which is a fair measure of the nonlinearity of the resonator.

Table 2.1: Summary of different capacitive-transduction MEMS resonators

Device	Configuration	Q	R_m(kΩ)
CC beam [61]		8000 @10MHz(vac.) 50 @10MHz(air) 300 @70MHz(vac.) Limited freq. range	8.7 @54.2MHz 35.2 @71.8MHz
FF beam [78]		20k @10-200MHz(vac.) 2k @90MHz(air) Wide freq. range	31.1 @31.51MHz 10.7 @50.35MHz 167 @92.25MHz
WG disc [76]		156k @60MHz(vac.) 8k @98MHz(air) Wide freq. range	176 @425.3MHz 200 @1500MHz
CM disc [64]		11.5k @1.5GHz(vac.) 10.1k @1.5GHz(air) Wide freq. range	480 @151.3MHz 2422 @1156MHz
HD ring [79]		11.5k @1.5GHz(vac.) 10.1k @1.5GHz(air) Wide freq. range	480 @151.3MHz 2422 @1156MHz
WG ring [70]		3k @1.5GHz(air) 7.7k @210MHz(air) Wide freq. range	600 @634MHz 791 @1.5GHz
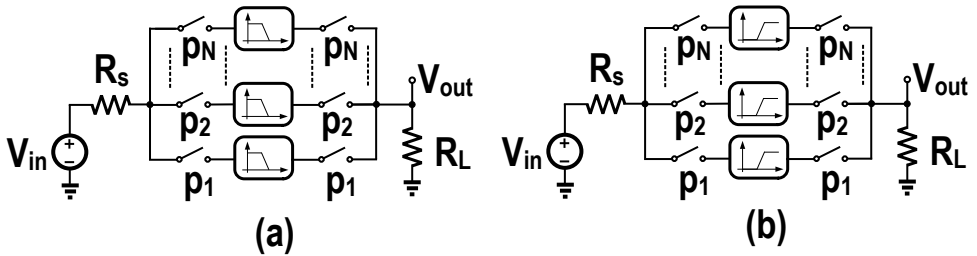
Figure 2.18: A general N-path (a) BPF (b) BSP.

However, RF frequency capacitive-transduction MEMS filters, having $S_{21} < -80$ dB, seem to be not viable options for RF filtering.

2.5   N-path Filters

N-path filtering is an old technique [81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91] (Fig. 2.18). The oldest N-path filter (at that time, it was called "commutated networks") seems to be [81] which was published in 1953. A center-frequency tunable switched-RC BPF and a band stop filter (BSF) were proposed in [81]. Interestingly, at that time, the switches were made mechanically due to the lack of transistors. The general idea of N-path filtering is simple. Instead of filtering the signal at RF, it is first downconverted to baseband by exploiting the first set of switches that operates as a mixer. Afterwards, these down-converted signals are lowpass (highpass) filtered due to the LP(HP) filters. Eventually, these filtered signals are upconverted again to the RF frequency. This procedure can be interpreted as a transformation of a LP(HP) filter to a BP(BS) filter around the switching frequency. This idea is usually very helpful because the design of LP(HP) filters is much easier than the design of BP(BS) filters. A time-domain analysis of general N-path filters has been presented in [82, 83, 85, 87, 89, 90] and a frequency-domain analysis of N-path filters was introduced in [83]. The first integrated N-path filters were demonstrated in [84, 86, 91]. The N-path technique was utilized in switched-capacitor filters extensively [87, 92, 93, 94]. At that time, the two main obstacles in the implementation of integrated N-path filters were: 1) the achievable matching between the different paths of the N-path filters, which is crucial for the proper operation of the filter, was not good enough [88]; and 2) the maximum achievable switching frequency of the integrated circuits was quite low. These two main issues reduced the attention of researchers for N-path filters. The substantial improvement in the speed and the matching properties of CMOS technology renewed a great interest into N-path filters [95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105]. Because the main constituents of N-path filters are switches and capacitors, CMOS
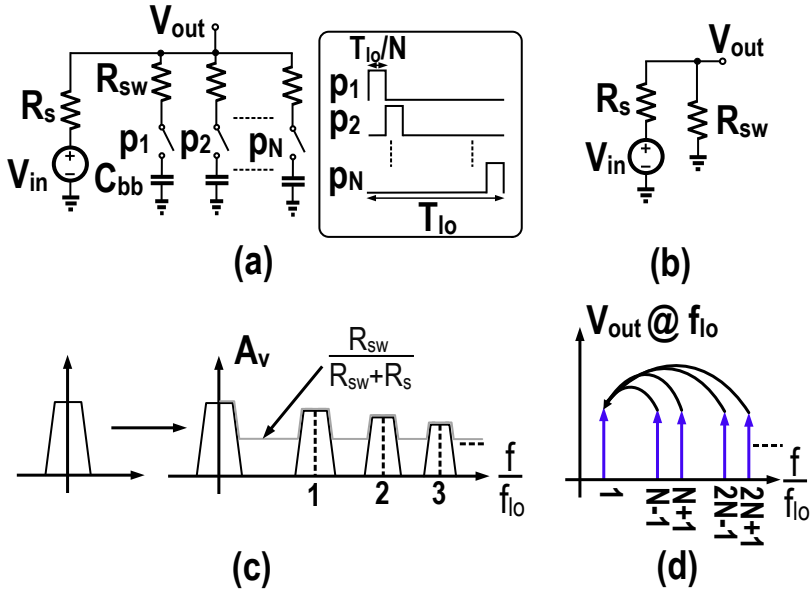
Figure 2.19: (a) An N-path BPF [81] (b) A simplified schematic of the filter for out-of-band frequencies (c) Transformation of a LPF to BPFs at different harmonics of the clock frequency, f_{lo}; non-zero R_{sw} limits the stopband rejection of the filter (d) Folding-back of Signals located at $|kN - 1|f_{\mathrm{lo}}$ to f_{lo}.

technology is the best candidate for the realization of this type of filters.

An N-path BPF [81] that has recently attracted much attention [95, 96, 97, 98, 99, 101, 102, 103, 104, 105] is illustrated in Fig. 2.19(a) where the on-resistance of the switches is modeled by a series resistance, R_{sw}. The clock signals, $p_i(t)$ $i = [1, \mathrm{N}]$, are non-overlapping clocks with a duty cycle of $1/\mathrm{N}$. The input RF signals located around the $\mathrm{m^{th}}$ harmonics of the clock frequency, mf_{lo}, will be downconverted to baseband due to the switching operation of the switches. These baseband signals are then filtered due to the lowpass filtering of the combination of baseband capacitors, C_{bb}, and the source resistance, R_s. Due to the transparency of the switches, these lowpass filtered baseband signals will be upconverted to around mf_{lo}. This procedure can be interpreted as a transformation of a LPF, which consists of C_{bb} and R_s, to BPFs centered at different harmonics of f_{lo}. The LPF to BPF transformation is illustrated in Fig. 2.19(c). In this way, N-path filters provide us with center-frequency tunable BPF where the bandwidth of the filter can be chosen independent of the center frequency by the value of C_{bb}. There are some issues associated with N-path filters, namely: 1) *limited stopband rejection* due to the non-zero switch resistance, R_{sw}; 2) *undesired folding-back* of the signals located at $|kN - 1|f_{\mathrm{lo}}$ to the center frequency of

the filter, f_{lo} (Fig. 2.19(d)); and 3) *the repetition of the bandpass shapes* at higher harmonics of the clock frequency. For frequencies far from the passband of the filter, the impedance of the baseband capacitors, C_{bb}, is negligible and can be ignored. In this way, the filter can be simplified to a resistive divider shown in Fig. 2.19(b). As a consequence, the ultimate-rejection of the filter is limited to $R_{sw}/(R_{sw} + R_s)$ as depicted in Fig. 2.19(c) [98].

2.6 Conclusion

The trend towards reconfigurable radio transceiver architectures asks for BPFs with good selectivity and a flexibly tunable center frequency. The off-chip available solution is to use an array of dedicated, bulky, off-chip and non-tunable filters such as SAW filters. Although BAW filters [53] have been introduced as a system in package solutions, their center frequency is sensitive to the thickness variation of the piezoelectric material and the achievable tunability is quite limited [53]. If they are used for reconfigurable receivers, an array of them is necessary which again leads to the usage of a considerable amount of area. On the other hand, there are several techniques to make integrated RF BPFs such as LC filters [14, 20, 21], often with Q-enhancement techniques, G_m-C filters [9, 14, 42], N-path filters [83, 87, 92, 93, 94, 103]. LC filters have several disadvantages such as high area consumption due to inductors which do not obey process scaling and have low quality factor, limited tunability and poor dynamic range [14, 20, 21]. The main drawbacks of G_m-C filters are the tradeoffs among power consumption, quality factor, center frequency and dynamic range and the need for tuning circuitry [14, 42]. On the other hand, N-path filters have interesting features such as direct tunability with f_{lo}, potentially higher Q-factors compared to the on-chip CMOS LC filters, high linearity and graceful scaling with process.

According to [14], the DR of G_m-C filters depends on $1/Q^2$ while the DR of the Q-enhancement filters depends on Q_0^2/Q^2 where Q_0 is the quality factor of on-chip inductors. G_m-C filters need extra circuitry (gyrators) to synthesize inductors and Q-enhancement filters require extra circuitry (a negative impedance) to enhance the Q-factor of on-chip inductors and these extra circuitries lead to a lower DR. However, in the N-path technique, the required Q-factor of the filter can be obtained by increasing C_{bb} ($Q \propto C_{bb}(R_s + R_{sw})$) and no extra active devices are needed. Therefore, essentially, the Q-factor of the N-path filters is decoupled from its DR. Therefore, the focus of this thesis is on the design and implementation of N-path filters.

Chapter 3

Tunable Switched G_m-C Bandpass Filter Based on N-path Filters

3.1 Introduction

As discussed in chapter 2, the trend towards reconfigurable radio transceiver architectures asks for BPFs with good selectivity and a flexibly tunable center frequency. As concluded in chapter 2, N-path filters are the best candidate for this purpose. A 4-path filter with capacitive baseband impedances and its LTI (Linear Time Invariant) equivalent around f_{lo} are depicted in Fig. 3.1(a) and Fig. 3.1(b), respectively [19, 96, 97, 101, 102, 106]. At frequencies far from f_{lo}, the baseband capacitors will be shorted to ground and thus the filter will be simplified to a simple resistive division between source resistance R_s and switch resistance R_{sw} [96] (Fig. 3.1(c)). N-path filters have two main limitations: 1) the switch resistance R_{sw} limits the ultimate rejection to $R_{sw}/(R_{sw}+R_s)$ where R_s is the source impedance (16 dB for $R_s = 50\ \Omega$ and $R_{sw} = 10\ \Omega$) [19, 96, 107]; 2) recently published N-path filters have only second order filtering, and higher orders have only been achieved by cascading [103], still rendering a "round"bandpass filter shape. In this chapter, a new method to increase the order of the bandpass filter while having a better passband shape compared to [103, 106] is proposed [99]. The introduced technique, also weakens the effect of the switch-resistance on the ultimate rejection obtaining > 55 dB ultimate rejection in a 65 nm LP CMOS chip.

The outline of this chapter is as follows: In section 3.2, the idea of subtraction as a method to obtain a 4th order BPF from two 2nd order BPFs with different center
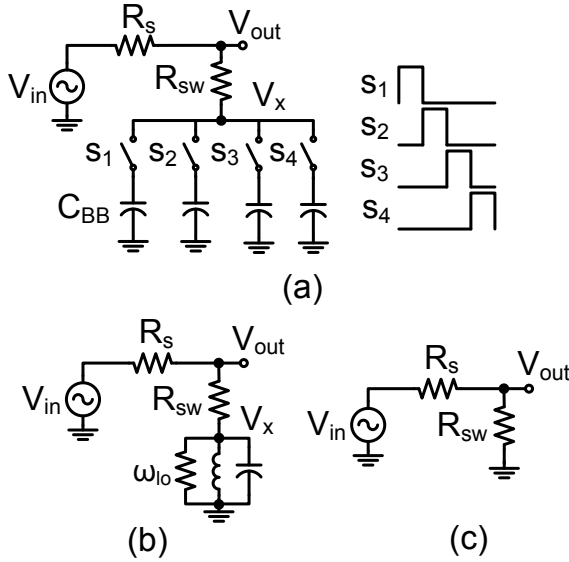
Figure 3.1: (a) A conventional 4-path filter (b) its LTI equivalent around f_{lo} and (c) equivalent circuit for evaluating the ultimate rejection.

frequencies will be introduced. Subsequently, in section 3.3 the idea of shifting the center frequency of a 4-path filter upward and downward exploiting a switched G_m-C technique will be discussed. Moreover, we discuss how the frequency shifts are implemented using a switched G_m-C technique. Consequently, utilization of this idea into the subtraction circuit, will be discussed. In Section 3.4, signal splitting to supply the input voltage signal to the two shifted 4-path 2nd order BPFs and its effect on the resultant filter will be discussed. Section 3.5 and 3.6 discuss the filter realization and measurements, respectively. In section 3.7, conclusions will be drawn.

3.2   Increasing BPF Order By Subtraction

We propose to use subtraction as a means to achieve a 4th order BPF from the two 2nd order BPFs with slightly different center frequencies. The main idea is illustrated in Fig. 3.2. Intuitively, the relation between the phase of V_{out1} and V_{out2} (ϕ_1 and ϕ_2) is approximately $\phi_1 = -\phi_2$ in the pass-band of the resultant filter and therefore due to the subtraction, they will add up. However, for frequencies far out of the pass-band region of the resultant filter, the signals in the 2 paths are almost in-phase $\phi_1 = \phi_2$ and will cancel each other. Mathematically, the transfer function of each path in Fig. 3.2 is:
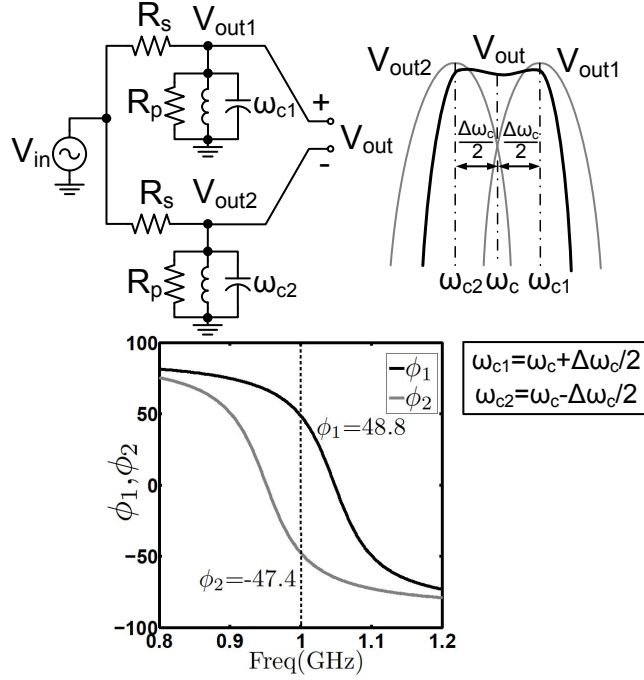
Figure 3.2: Obtaining a 4th order BPF based on the subtraction of two 2nd order BPFs with slightly different center frequencies; the relation between the phase of each path (ϕ_1,ϕ_2): in the pass-band of the resultant filter is approximately $\phi_1 = -\phi_2$ and for frequencies far out of the pass-band region of the resultant filter, the signals in the 2 paths are almost in-phase ($\phi_1 = \phi_2$).

$$H_i(s) = \frac{V_{\text{out},i}(s)}{V_{\text{in}}(s)} = \frac{R_p}{R_s + R_p} \times \frac{\omega_{3\text{dB},i}s}{s^2 + \omega_{3\text{dB},i}s + \omega_{ci}^2} \quad i = 1, 2 \qquad (3.1)$$

where ω_{ci} and $\omega_{3\text{dB},i}$ are center frequencies and bandwidths of the two paths. If the bandwidth of each path is the same ($\omega_{3\text{dB},1} = \omega_{3\text{dB},2} = \omega_{3\text{dB}}$) and assuming that $\omega_{c1} = \omega_c + 0.5\Delta\omega_c$ and $\omega_{c2} = \omega_c - 0.5\Delta\omega_c$, the total transfer function of the resultant filter will be:

$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{R_p}{R_s + R_p} \times \frac{2\omega_{3\text{dB}} \times \omega_c \times \Delta\omega_c \times s}{(s^2 + \omega_{3\text{dB}}s + \omega_{c1}^2)(s^2 + \omega_{3\text{dB}}s + \omega_{c2}^2)}. \qquad (3.2)$$

Now, we want to synthesize a 4th order BPF which has a bandwidth of BW(Hz) and is centered at ω_c. Let us assume that the desired LPF prototype is $k/(s^2 + as + b)$.
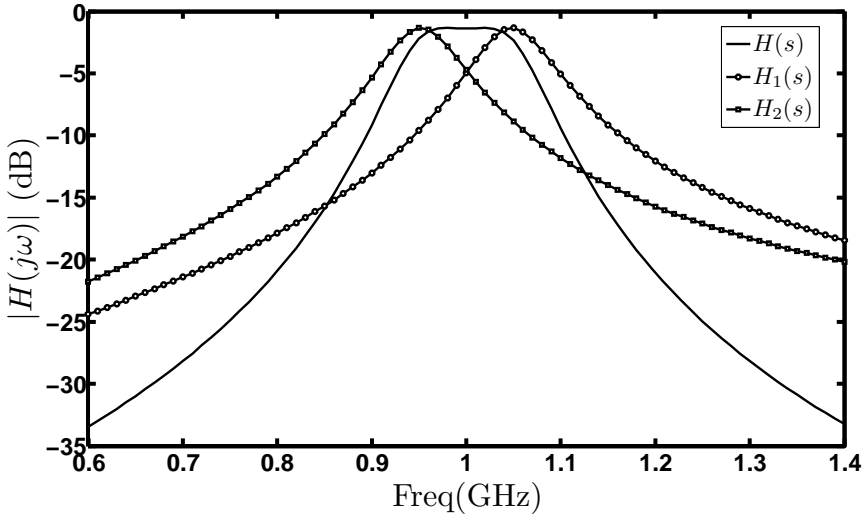
Figure 3.3: A 4$^{\text{th}}$ order BPF centered at $f_c = 1$ GHz with BW = 124 MHz and 0.05 dB ripple ($a = 0.7$, $b = 0.27$) centered at 1 GHz as a result of the subtraction of two 2$^{\text{nd}}$ order BPFs with bandwidths of 87 MHz centered at $f_{c1} = 1.05$ GHz and $f_{c2} = 0.95$ GHz (R$_s$ = 50 Ω and R$_p$ = 300 Ω).

For this purpose, the values needed for $\Delta\omega_c$ and $\omega_{3\text{dB}}$ are 2πBW $\times \sqrt{4b - a^2}$ and 2πBW $\times a$, respectively. For example, by subtracting the outputs of two 2$^{\text{nd}}$ order BPFs with bandwidth of 87 MHz centered at $f_{c1} = 1.05$ GHz and $f_{c2} = 0.95$ GHz, a 4$^{\text{th}}$ order BPF centered at $f_c = 1$ GHz with 0.05 dB ripple and bandwidth of 124 MHz will result (Fig. 3.3).

Each RLC tank in Fig. 3.2 can be replaced by a 4-path passive-mixer filter with different clock frequencies (f_{c1} and f_{c2}, one for each path). In this way, a tunable 4$^{\text{th}}$ order BPF can be made (Fig. 3.4(a)). Another property of this filter is that it can improve the limited ultimate rejection of conventional N-path filters. The filter shown in Fig. 3.4(a) will reduce to Fig. 3.4(b), for input frequencies far from the center frequency of the filter. In the case of no mismatch in the subtraction and the switch resistance values of upper and lower paths, the ultimate rejection will be infinite (R$_{sw}$/(R$_{sw}$ + R$_s$) $-$ R$_{sw}$/(R$_{sw}$ + R$_s$)=0). In case of switch resistance mismatch ΔR$_{sw}$ between upper and lower path, the ultimate rejection will be limited to ΔR$_{sw}$/(R$_{sw}$ + R$_s$). Compared to the ultimate rejection of conventional N-path filters, a great improvement has been introduced. For example for a 1% mismatch between the switch resistance values of the upper and lower path and assuming R$_{sw}$ = 10 Ω and R$_s$ = 50 Ω, the ultimate rejection will be 55 dB compared to 16 dB ultimate rejection of conventional N-path filters. A disadvantage of the filter shown in Fig.
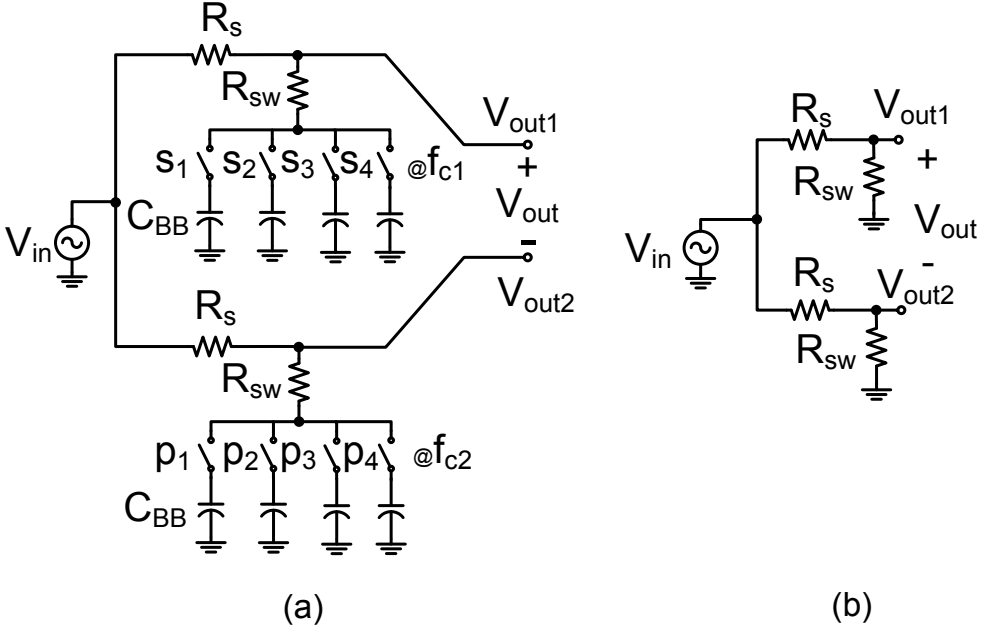
Figure 3.4: (a) A 4th order tunable BPF using two different clock frequencies and (b) equivalent circuit to find the ultimate rejection

3.4(a) is the need for a complicated clock circuitry. Instead, an alternative way is proposed to realize the filter with just one clock frequency which is discussed in section 3.3.

3.3 Shifting the center frequency of a 4-path filter

The idea of shifting the center frequency of the 4-path filter with respect to the switching frequency f_{lo} using a G_m-C technique is illustrated in Fig. 3.5. The idea of shifting the center frequency of a 4-path filter has recently also been proposed independently in [101]. By exploiting the poly-phase signals in the baseband of a 4-path filter, its center frequency can be changed upward or downward with respect to the clock frequency. By doing a clockwise and counter clockwise feeding of the g_m cells to the baseband nodes (V_{bi}, $1 \leq i \leq 4$) of a 4-path filter with capacitive baseband impedances, the center frequency of the filter is changed to $f_{\text{lo}} + g_m/(2\pi C_{\text{BB}})$ and $f_{\text{lo}} - g_m/(2\pi C_{\text{BB}})$, respectively. Consequently, the upper and lower path of the filter depicted in Fig. 3.4(a) can be substituted by the circuits shown in Fig. 3.5(a) and (b), respectively. In this way instead of two different clock frequencies, one clock
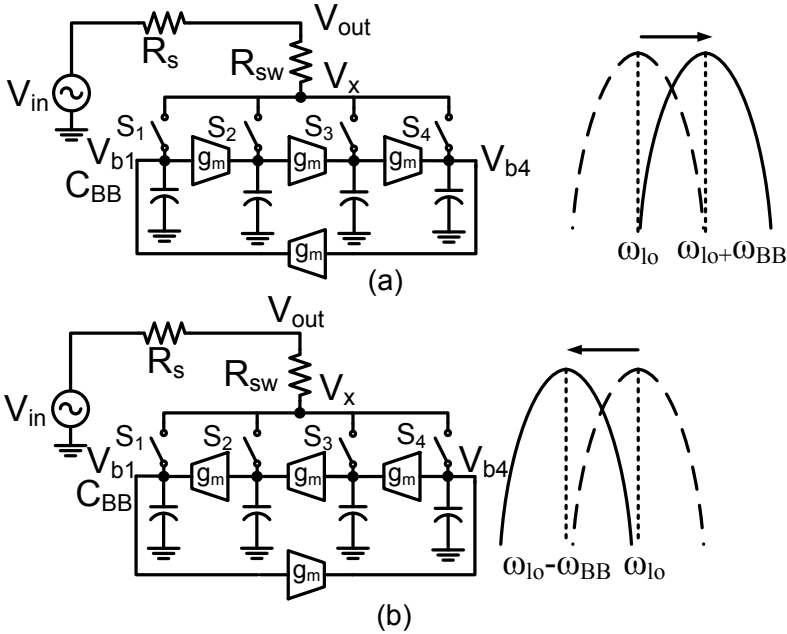
Figure 3.5: Clockwise and counter clockwise feeding of the g_m cells in baseband nodes to shift the center frequency of a 4-path filter a) upward and b) downward compared to ω_{lo} by $\omega_{\mathrm{BB}} = g_m/C_{\mathrm{BB}}$.

frequency will suffice. This is a great advantage, because considering two slightly different clock frequencies on an IC will cause serious interference problems.

When f_{in} is around kf_{lo}, the phase relation between the voltages of baseband nodes $V_{bi}(1 \leq i \leq 4)$ of a 4-path filter can be described by $V_{bm} = V_{bn}e^{+jk\pi/2\times(m-n)}$, $(1 \leq (m,n) \leq 4)$. By exploiting that, the interactions between the baseband nodes due to the g_m cells in filters shown in Fig. 3.5 can be lumped to an effective baseband admittance $Y_{\mathrm{BB}}(s,k)$ when the input frequency is around kf_{lo}.

$Y_{\mathrm{BB}}(s,k)$ for f_{in} around kf_{lo} ($1 \leq k \leq 3$) for the filter shown in Fig. 3.5(a) is illustrated in Fig. 3.6(a). From Fig. 3.6(a), $Y_{\mathrm{BB}}(s,1) = C_{\mathrm{BB}}(s - j\omega_{\mathrm{BB}})$, $Y_{\mathrm{BB}}(s,2) = sC_{\mathrm{BB}} - g_m$ and $Y_{\mathrm{BB}}(s,3) = C_{\mathrm{BB}}(s + j\omega_{\mathrm{BB}})$, where ω_{BB} is g_m/C_{BB} (In the same way the filter shown in Fig. 3.5(b) can be analyzed). Therefore the center frequency of the baseband admittance is modified from zero to ω_{BB} for $Y_{\mathrm{BB}}(s,1)$ and $-\omega_{\mathrm{BB}}$ for $Y_{\mathrm{BB}}(s,3)$, however for $Y_{\mathrm{BB}}(s,2)$, the center frequency of the baseband admittance does not change. In N-path filters, the baseband admittance characteristics will be translated to kf_{lo} $k \in \mathbb{Z}$ [83, 87, 102]. This means that the center frequency of the filter shifts upward around f_{lo} and downward around $3f_{\mathrm{lo}}$ by $g_m/(2\pi C_{\mathrm{BB}})$. The situation is different around $2f_{\mathrm{lo}}$ in which the center frequency does not change. Instead the g_ms
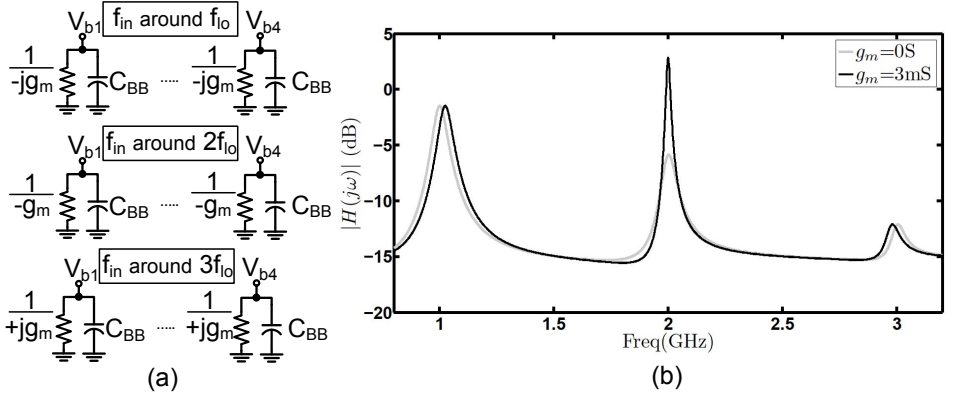
Figure 3.6: (a) Effective baseband admittance $Y_{BB}(s,k)$ ($1 \leq k \leq 3$) for filter shown in Fig. 3.5(a), voltages V_{bi} ($1 \leq i \leq 4$) are the baseband nodes of the filter; and (b) SpectreRF simulation of Fig. 3.5(a) with $g_m = 0$ mS and 3 mS ($R_s = 50$ Ω, $R_{sw} = 10$ Ω, $C_{BB} = 20$ pF and $f_{lo} = 1$ GHz).

create a negative resistance, $-1/g_m$, in parallel with each baseband capacitor which leads to an increase in the passband gain and reduction of bandwidth at $2f_{lo}$. This behavior is shown in Fig. 3.6(b).

It is found that exploiting the differential G_ms ($G_m = 0.5$ g_m) with good common-mode rejection can prevent the creation of this negative resistance[1] at $2f_{lo}$. Exploiting the differential G_ms is illustrated in Fig. 3.7. The filter with the differential G_ms acts the same as the one with the single-ended g_ms for input frequencies around f_{lo} and $3f_{lo}$, however for input frequencies around $2f_{lo}$ because of the fact that $V_{b1} = V_{b3}$ and $V_{b2} = V_{b4}$, the output current of both differential G_ms will be diminished to zero ($G_m(V_{b1} - V_{b3}) = G_m(V_{b2} - V_{b4}) = 0$). As a result, there will be no effect from the differential G_ms and the filter operates similar to a conventional 4-path filter for input frequencies around $2f_{lo}$. The frequency shifting with single-ended and differential transconductances has been compared in Fig. 3.8 (see section 3.5). As can be seen, exploiting the differential G_ms suppresses the positive feedback at even harmonics of f_{lo}. Fig. 3.9 shows a tunable 4th order BPF based on the subtraction of two 2nd order BPFs whose center frequencies are shifted upward and downward relative to f_{lo} using the differential G_m cells. Additionally, a second set of switches has been added to each path to increase the ultimate rejection of each path. In this way, node V_x instead of node V_{out} in Fig. 3.5 (a) and (b) is exploited. Therefore the ultimate rejection of the filter will be much less prone to the mismatch in the subtraction circuitry and switches. As mentioned before, there is no contribution from

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[1]The condition for the stability is $g_m \leq 1/(4(R_s + R_{sw}))$.
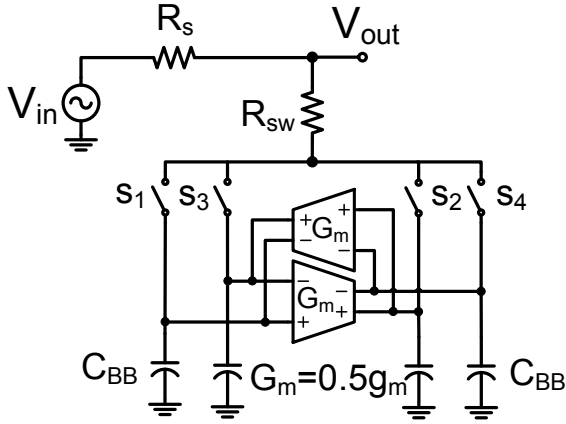
Figure 3.7: Using the differential G_ms with good common-mode rejection instead of the single-ended ones to shift the center frequency of 4-path filter upward
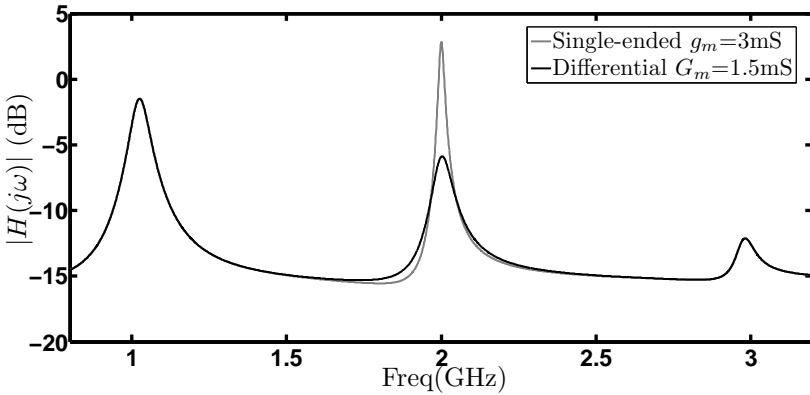
Figure 3.8: SpectreRF simulation of Fig. 3.5(a) with $g_m = 3$ mS and Fig. 3.7 with $G_m = 1.5$ mS ($R_s = 50\ \Omega$, $R_{sw} = 10\ \Omega$, $C_{BB} = 20$ pF and $\omega_{lo} = 1$ GHz).

the differential G_ms at $2f_{lo}$ in both paths. As a result, both paths operate similar to each other and accordingly the band-pass filter shape at $2f_{lo}$ will be suppressed due to the subtraction (Fig. 3.10). Using (3.15), we can calculate the transfer function of the filter around f_{lo} (3.3). $G(s, k)$ is a LPF due to the combination of the baseband and source admittances which due to the transparency of the switches is translated to a BPF around kf_{lo}. The transfer function of the filter around f_{lo} can be found by using two terms($k = -1, 1$) of (3.15).
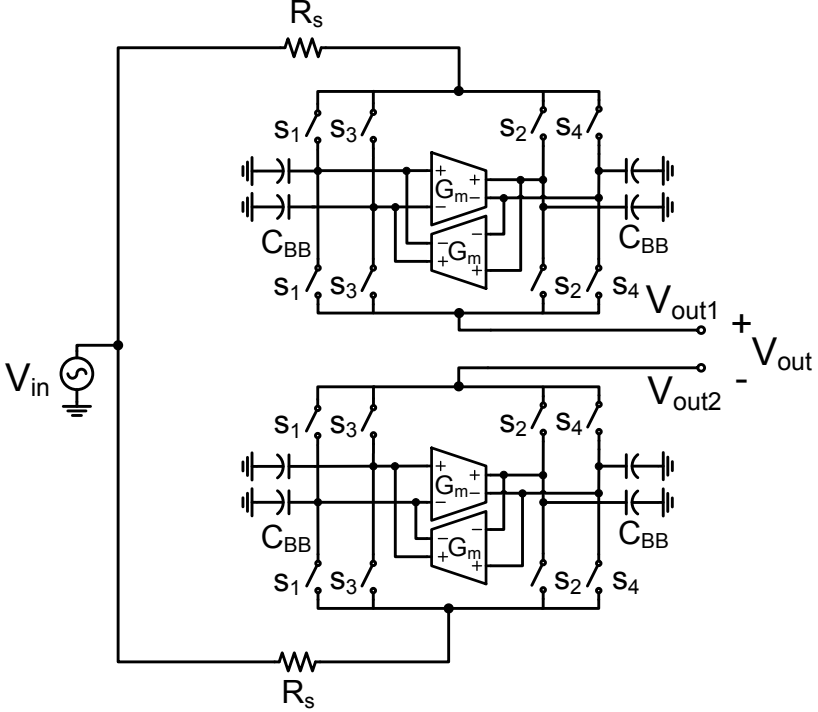
Figure 3.9: A 4th order tunable BPF by the subtraction of two 2nd order BPFs which their center frequencies have been shifted upward and downward relative to f_{lo} ($G_m = 0.5\, g_m$) using switched G_m-C technique; a second set of switches has been added to each path to increase the ultimate rejection of each path.

$$T_1(s) = \frac{V_{\text{out1}}(s)}{V_{\text{in}}(s)} = \frac{8}{\pi^2} \times (G(s - j\omega_{\text{lo}}, 1) + G(s + j\omega_{\text{lo}}, -1)) \qquad (3.3)$$

Where $G(s, \pm1)$ is:

$$G(s, \pm1) = \frac{1}{1 + 4R_x Y_{\text{BB}}(s, \pm1)} = \frac{1}{1 + 4R_x(sC_{\text{BB}} \pm jg_m)} \qquad (3.4)$$

and R_x is $R_s + R_{sw}$. Subsequently, $T_1(s)$ will be:

$$
\begin{aligned}
T_1(s) &= \frac{8}{\pi^2} \times \left(\frac{1}{1 - j4g_m R_x + 4R_x C_{\text{BB}}(s - j\omega_{\text{lo}})} \right) \\
&+ \frac{8}{\pi^2} \times \left(\frac{1}{1 + j4g_m R_x + 4R_x C_{\text{BB}}(s + j\omega_{\text{lo}})} \right) \\
&= \frac{8}{\pi^2} \times \frac{s/(2R_x C_{\text{BB}})}{s^2 + s/(2R_x C_{\text{BB}}) + (\frac{g_m}{C_{\text{BB}}} + \omega_{\text{lo}})^2}
\end{aligned}
\qquad (3.5)
$$
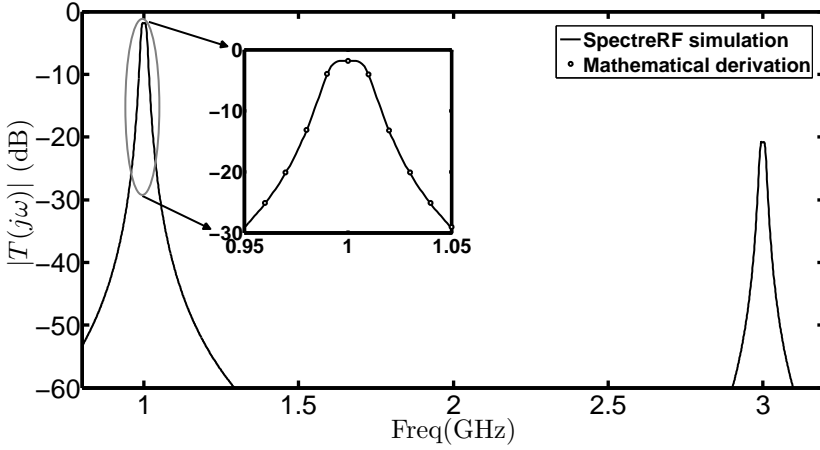
Figure 3.10: Comparing SpectreRF simulation of the filter shown in Fig. 3.9 with mathematical derivation (3.6) for a 4th order BPF with bandwidth of 20 MHz ($a = 0.7$, $b = 0.27$) centered at 1 GHz ($R_s = 50\Omega$, $R_{sw} = 10 \ \Omega$, $G_m = 2.3$ mS and $C_{BB} = 95$ pF) and demonstration of the suppression of bandpass filtering at even harmonics of f_{lo}.

$T_2(s)$ can be easily found by changing g_m to $-g_m$ in (3.5). Then, the total transfer function of the filter ($T(s) = T_1(s) - T_2(s)$) is described by (3.6) where $\omega_{c1} = \omega_{lo} + g_m/C_{BB}$ and $\omega_{c2} = \omega_{lo} - g_m/C_{BB}$. To synthesize a 4th order BPF with bandwidth of BW(Hz) which is centered at ω_{lo} and assuming that the desired LPF prototype is $k/(s^2+as+b)$, the values needed for C_{BB} and g_m are $\frac{1}{4\pi a R_x \times BW}$ and $\frac{1}{4R_x} \times \sqrt{4b/a^2 - 1}$, respectively. The bandwidth of the filter can be tuned by changing the value of C_{BB} while the value of G_m is constant. This feature can be used to accommodate multiple standards. For example, for $R_s = 50 \ \Omega$ and $R_{sw} = 10 \ \Omega$, a tunable 4th order BPF with bandwidth of 20 MHz will result for $C_{BB} = 95$ pF and $G_m = 2.3$ mS (Fig. 3.10). Moreover, Fig. 3.10 shows the suppression of BPFs at even harmonics of f_{lo}.

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = T_1(s) - T_2(s)$$
$$= \frac{16}{\pi^2} \times \frac{g_m \omega_{lo}}{R_x C_{BB}^2} \times \frac{s}{\left(s^2 + \frac{s}{2R_x C_{BB}} + \omega_{c1}^2\right)\left(s^2 + \frac{s}{2R_x C_{BB}} + \omega_{c2}^2\right)} \quad (3.6)$$

3.4 Splitting the input signal

In practice, the output resistance of V_{in} is not zero and this leads to an interaction between the two paths which is undesirable and will impact the transfer function of
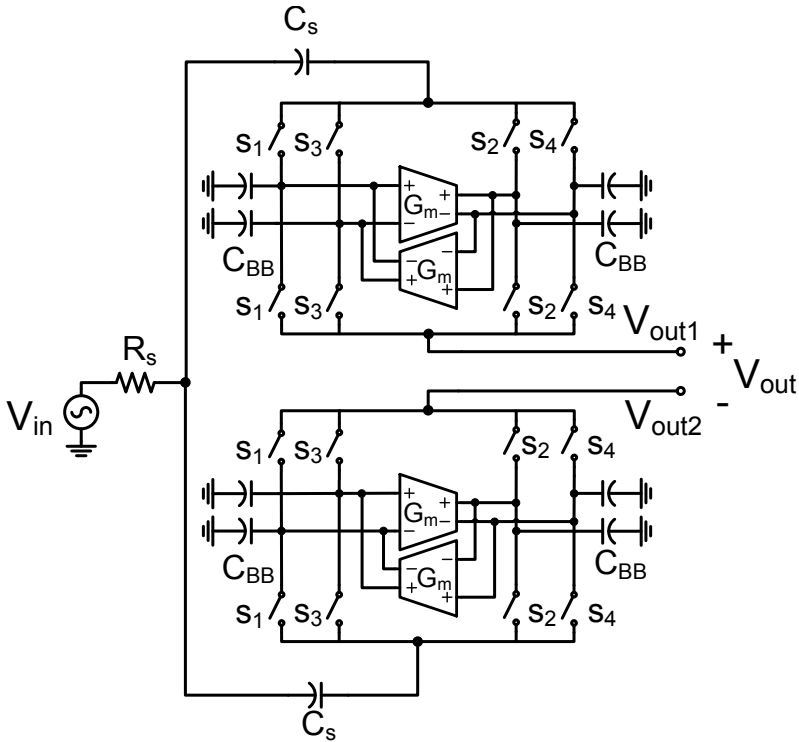
Figure 3.11: Splitting the input signal and providing isolation between the two paths by using in each path a capacitance with a relatively high impedance at the frequencies of interest, compared with the impedance R_s.

the filter. Therefore, it is needed to split the input voltage to each path while having as little interaction as possible between the two paths. There are several options to do this. For example, two amplifiers can be exploited for this purpose but this limits the linearity of the filter. The next possibility is using the time domain signal splitting by series switches with each path which are clocked by two anti-phase clock signals at $4f_{lo}$. For the proper operation of the filter in the time domain signal splitting, the clock signals of one path need to be shifted by $T_{lo}/8$ compared to the clock signals of the other path which complicates the clock circuitry. Another option is to use relatively high capacitive impedances compared to the source resistance (Fig. 3.11). Although it leads to an increase in the NF of the filter, exploitation of the series capacitors is chosen due to its simplicity and considerable increase in the quality factor of the filter compared to the other approaches. Therefore the filter shown in Fig. 3.11 will be the implemented filter.

3.4.1 The effect of series capacitor on a conventional 4-path filter

First, the effects of addition of a series capacitor to each path in Fig. 3.11 individually while assuming $G_m = 0$ will be investigated. Intuitively, due to the fact that the input impedance of a 4-path filter imitates a parallel RLC tank, the addition of a series capacitor acts as an L-match section [25] and effectively increases the quality factor and the voltage gain of the filter. Moreover from Appendix 3.B, $V_{out1,2}/V_{in}$ in Fig. 3.11 by assuming that $\tau_s \omega_{lo} < 0.5$ ($\tau_s = R_x C_s$) and neglecting the mutual loading effect of each path on the other one[2], will be:

$$\mathrm{T}(s) = \frac{\mathrm{V_{out1,2}}}{\mathrm{V_{in}}} \cong \frac{8}{\pi^2} \times \frac{\tau_s s}{1 + \tau_s s}$$
$$\times \frac{s/(2\mathrm{R}_x \mathrm{C_{BB}})}{s^2 + (\mathrm{C}_s \omega_{lo}/(\pi \mathrm{C_{BB}}))s + \omega_{lo}^2 \times (1 - \mathrm{C}_s/(\pi \mathrm{C_{BB}}))} \quad (3.7)$$

The $|\mathrm{T}|_{max} \cong 4/\left(\pi\sqrt{1 + \tau_s^2 \omega_{lo}^2}\right)$ occurs at $f_c \cong f_{lo} \times [1 - 0.5\mathrm{C}_s/(\pi \mathrm{C_{BB}})]$. As an example, for $\mathrm{R}_s = 50\ \Omega$, $\mathrm{R}_{sw} = 10\ \Omega$, $\mathrm{C_{BB}} = 20$ pF, $\mathrm{C}_s = 1$ pF and $f_{lo} = 1$ GHz, the center frequency of the filter will be $f_c = 992$ MHz and the maximum gain will be $\mathrm{A}_{v,max} = 1.5$ dB (Fig. 3.12). As can be seen, the gain has been increased by approximately 3.3 dB compared to a conventional 4-path filter. The quality factor of the filter can be approximated by $Q \cong \pi \mathrm{C_{BB}}/\mathrm{C}_s - 2$. The improvement in Q can be significant, e.g. from 15 to 60 for the case given in Fig. 3.12. Also shown in Fig. 3.12 is a comparison between the calculated filter shape (3.7) and the simulation.

The NF at node $V_{out1,2}$ for frequencies around f_{lo} by assuming that $\tau_s \omega_{lo} < 0.5$, $G_m = 0$ and neglecting the noise contribution of the second set of switches and loading effect of each path on the other one, is described in (3.8) (see (3.23)).

$$\mathrm{F}(\omega) \cong \frac{\pi}{4} \times \left(1 + \frac{\mathrm{R}_{sw}}{\mathrm{R}_s}\right) \times \left(\omega_{lo}\tau_s + \frac{1}{\omega_{lo}\tau_s} \times \left(\frac{\omega_{lo}}{\omega}\right)^2\right) \quad (3.8)$$

For $\mathrm{R}_s = 50\ \Omega$, $\mathrm{R}_{sw} = 10\ \Omega$, $\mathrm{C_{BB}} = 20$ pF, $\mathrm{C}_s = 1$ pF and $f_{lo} = 1$ GHz, the NF of the filter is approximately 4.5 dB. Despite the increase in voltage gain due to the usage of a series capacitor, the NF of the filter increases compared to a conventional 4-path filter. Simulations correspond to calculations within 0.2 dB.

3.4.2 Transfer function of the implemented filter

In the presence of a frequency shift due to the G_m cells, the transfer function shown in (3.7) needs to be modified. It is just needed to change ω_{lo} to $\omega_{lo} + g_m/\mathrm{C_{BB}}$ and

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[2]Removing the other path.
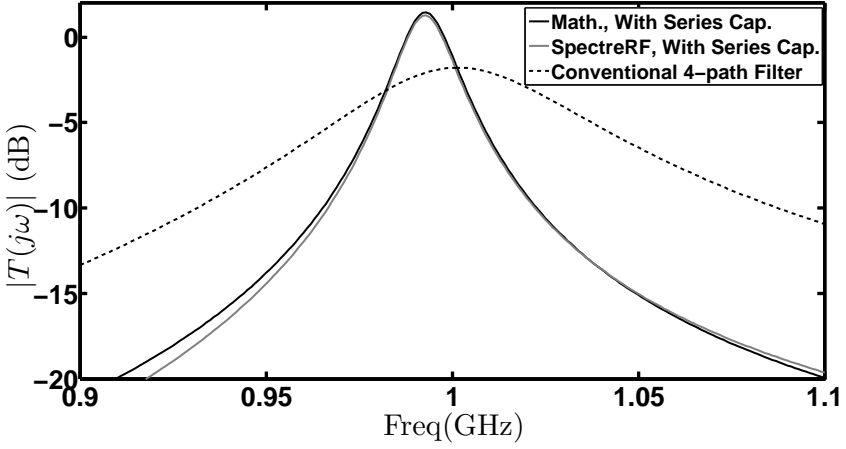
Figure 3.12: SpectreRF simulation of one path in Fig. 3.11 with and without a series cap, $C_s = 1$ pF, while $G_m = 0$ and the other path is removed compared with mathematical derivation (3.7); $R_s = 50$ Ω, $R_{sw} = 10$ Ω, $C_{BB} = 20$ pF and $f_{lo} = 1$ GHz.

$\omega_{lo} - g_m/C_{BB}$ in (3.7) to find $T_1(s) = V_{out1}/V_{in}$ and $T_2(s) = V_{out2}/V_{in}$ in Fig. 3.11, respectively. By doing so, the total transfer function ($T = T_1 - T_2$) of the filter illustrated in Fig. 3.11 while neglecting the mutual loading effect of each path on the other one is described in:

$$
\begin{aligned}
T(s) = \frac{V_{out}(s)}{V_{in}(s)} &\cong \frac{16 g_m \omega_{lo} \left(1 - C_s/(\pi C_{BB})\right)}{\pi^2 C_{BB}^2 R_x} \times \frac{\tau_s s}{1 + \tau_s s} \\
&\times \frac{s}{(s^2 + \alpha s + \omega_{x1}^2) \times (s^2 + \alpha s + \omega_{x2}^2)}
\end{aligned}
\tag{3.9}
$$

Where $\omega_{x1} = (\omega_{lo} + g_m/C_{BB}) \times \sqrt{1 - C_s/(\pi C_{BB})}$, $\omega_{x2} = (\omega_{lo} - g_m/C_{BB}) \times \sqrt{1 - C_s/(\pi C_{BB})}$ and $\alpha = C_s \omega_{lo}/(\pi C_{BB})$. To synthesize a 4th order BPF with bandwidth of BW(Hz) which is centered at ω_c and assuming that the desired prototype LPF is $k/(s^2 + as + b)$, the values needed for C_{BB} and g_m are $\frac{C_s \omega_{lo}}{2a\pi^2 \times BW}$ and $\frac{C_s \omega_{lo}}{2\pi} \times \sqrt{4b/a^2 - 1}$, respectively.

Interestingly, reducing the series capacitance C_s lowers the required impedance level of the filter, and therefore the required values for C_{BB} and G_m for a certain bandwidth. To achieve a bandwidth of 20 MHz at 1 GHz while C_s is 1pF, the values of C_{BB} and G_m will be 20 pF and 0.5 mS, respectively. However without using C_s, the required values are 95 pF and 2.3 mS (Fig. 3.10). This means that the total value of the baseband capacitances reduces from 380 pF to 80 pF in each path. Nevertheless,
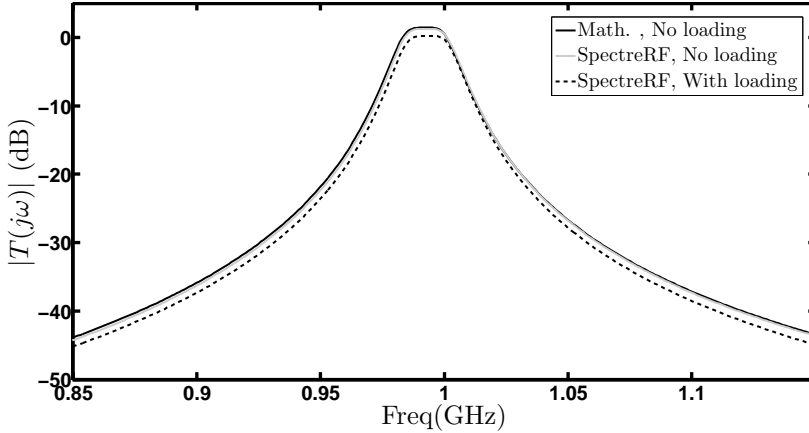
Figure 3.13: Comparing SpectreRF simulation of the filter shape with and without considering the mutual loading effect of each path on the other one with the derived equation (3.9) where the mutual loading effect is not taken into account; $R_s = 50\Omega$, $R_{sw} = 10 \ \Omega$, $C_{BB} = 20$ pF, $G_m = 0.5$ mS and $C_s = 1$ pF

there is a tradeoff between the reduction in the value of series capacitor C_s and the NF of the filter (see subsection 3.4.3). In Fig. 3.13 the simulated filter shape is compared with derived equation(3.9). As can be seen, the mutual loading effect[3] of each path on the other one leads to 1dB degradation in voltage gain in the pass-band of the filter. Because of the frequency dependency of the impedance of the series capacitors, two values of 1.7 pF and 1 pF are used for C_s for $f_c = 0.4$ GHz-0.7 GHz and $f_c = 0.7$ GHz-1.2 GHz, respectively. The simulated transfer function of the proposed filter for center frequencies from 0.4 GHz to 1.2 GHz is illustrated in Fig. 3.14. The maximum pass-band ripple is 0.6 dB.

It is interesting to mention that the same reduction in the baseband capacitance values can be achieved, if the series capacitors are substituted by series resistors. In this case, the required series resistance value in each path is around 200 Ω which leads to the noise figure of 9.3 dB while by utilizing the series capacitors, the noise figure of the filter will be 5.6 dB (see subsection 3.4.3).[4] Finally, it should be mentioned that the N-path filters much like any hard switching mixers [108] suffer from folding-back from harmonics of f_{lo} to the passband of the filter at f_{lo}[19]. Increasing the number of phases relaxes this issue (folding back begins from (N-1)f_{lo} where N is the number of phases [101]). Moreover, folding back from harmonics of the f_{lo}, can be eliminated by a time-invariant wideband and fixed low-pass pre-filter. The down-conversion of

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[3]The mutual loading effect of each path on the other one can be distinguished in the simulation by driving each path with a separate input voltage source.

[4]The noise contribution of the G_m cells is not taken into account.
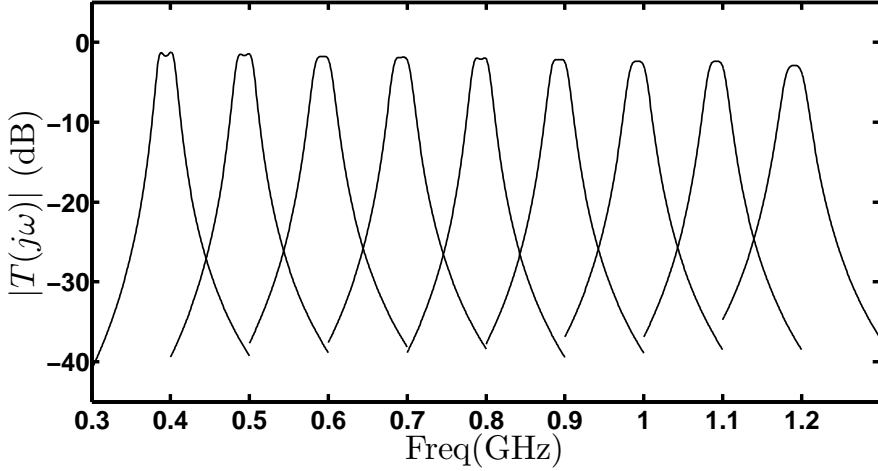
Figure 3.14: SpectreRF simulation of 4th order switched G_m-C BPF with bandwidth of 20MHz and ripple< 0.6 dB ($a = 0.76$, $b = 0.26$) from 0.4 GHz to 1.2 GHz; $R_s = 50\ \Omega$, $R_{sw} = 10\ \Omega$, $C_{\text{BB}} = 20$ pF, $G_m = 0.5$ mS and $C_s = 1$ pF and 1.7 pF.

up-converted baseband noise to harmonics of f_{lo} in the receiver can be eliminated by using a harmonic rejection mixer [108] or a time-invariant wideband low-pass post-filtering. The phase noise of the clock signals can increase the NF of the filter because of the reciprocal mixing of out-of-band interferers to the passband of the filter [102].
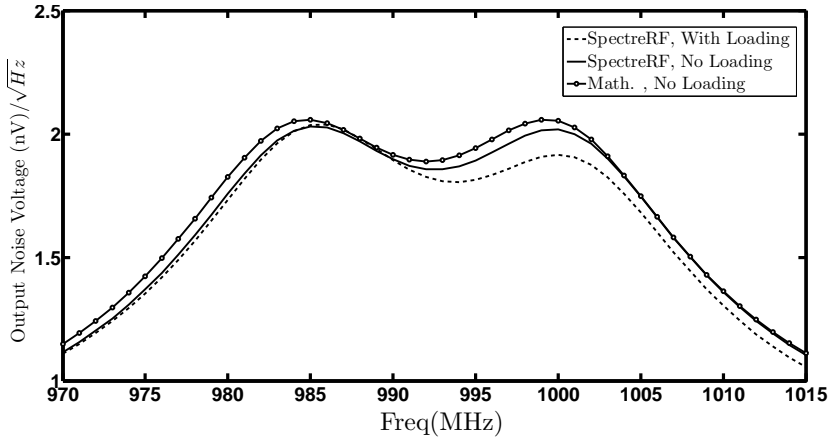
Figure 3.15: Comparing SpectreRF simulation of the output noise voltage of the filter shown in Fig. 3.11 with and without taking into account the mutual loading effect of each path on the other one with its mathematical derivation excluding the noise contribution of the G_m cells (3.24).
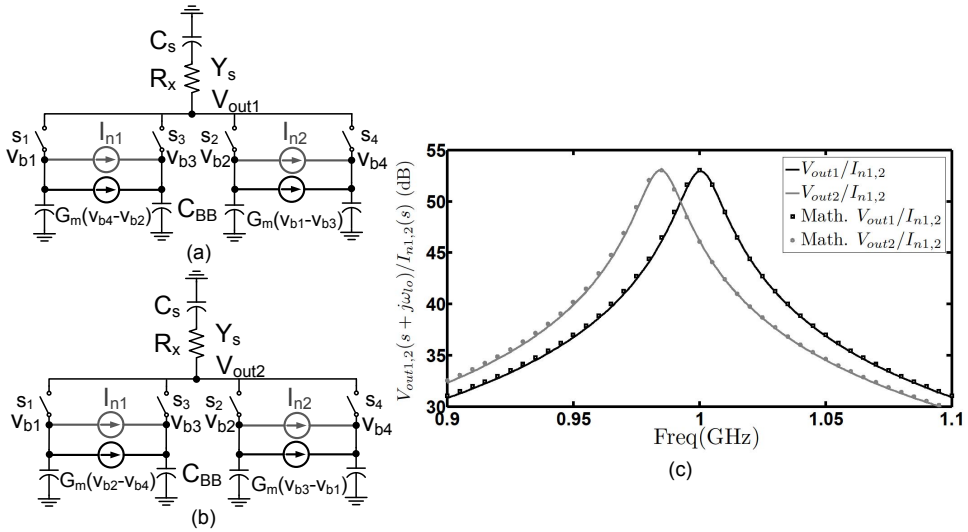
Figure 3.16: Circuits used to derive the transimpedance gain from $I_{n1,2}(s)$ to $V_{out1,2}(s + j\omega_{lo})$ for each path of the filter shown in Fig. 3.11 and (c) Comparing the SpectreRF simulation of the transimpedance gain of $V_{out1}/I_{n1,2}$ and $V_{out2}/I_{n1,2}$ with their mathematical derivations (see (3.27) and (3.28)), $R_s = 50 \, \Omega$, $R_{sw} = 10 \, \Omega$, $C_{BB} = 20 \, pF$, $C_s = 1 \, pF$, $G_m = 0.5 \, mS$ and $f_{lo} = 1 \, GHz$.

3.4.3 NF of the implemented filter

The output voltage noise of the filter illustrated in Fig. 3.11 excluding the noise contribution of the G_m cells is found in (3.24). In Fig. 3.15, A comparison between the SpectreRF simulation and the mathematically derived equation has been made. As can be seen, the SpectreRF simulation and the derived equation closely match and not taking into account the mutual loading effect of each path on the other path introduces less than 5% error. The NF of the filter, not taking into account the noise contribution of the G_m cells, is 5.6 dB. To take into account the noise contribution of the differential G_m cells, first the transfer function of the equivalent baseband current noises in each path (I_{n1}, I_{n2}) to the output of each path should be found (using the circuit shown in Fig. 3.16). Because of the limited bandwidth of the baseband nodes, only the low frequency contents of the baseband current noises are taken into account. A comparison between SpectreRF simulation and the derived equations (see (3.27) and (3.28)) for $V_{out1,2}(s + j\omega_{lo})/I_{n1,2}(s)$ of the filter has been made in Fig. 3.16(c). Consequently, the total NF of the filter will be (3.10) where F_1 (see (3.29)) is the noise figure of the filter without considering the noise contribution of the G_m cells and NEF_2 (see (3.30)) is the noise excess factor due to the differential G_m cells in
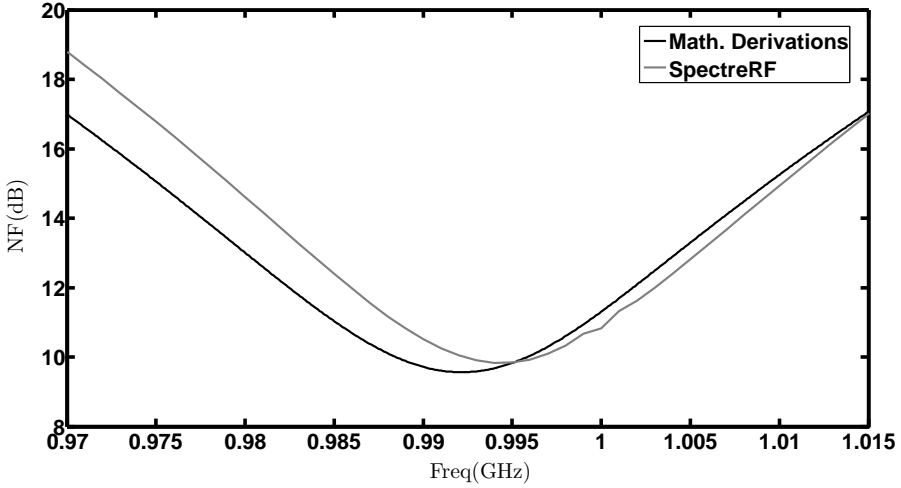
Figure 3.17: Comparing the SpectreRF simulation of the NF of the filter and its mathematical derivation (3.10) assuming a 1 dB voltage loss due to the mutual loading effect of each path one the other one.

both paths.

$$F = F_1 + NEF_2 \tag{3.10}$$

The equivalent output current noise of the differential G_m cells (Fig. 3.18(a)) can be estimated by $I_{nb}^2 \cong g_m^2/4 \times [8kT/g_m + 8kT/(R_p g_m^2)]$ where R_p is the degeneration resistance of the PMOS transistor in Fig. 3.18(a). The $1/f$ noise contribution of the G_m cells is heavily reduced by exploiting large transistors being heavily degenerated, which is possible thanks to using a high supply voltage for the baseband circuit since speed is not an issue here. A comparison between SpectreRF simulation of the total NF of the filter and its mathematical derivation (3.10) is illustrated in Fig. 3.17. The calculated and simulated NF of the implemented filter are 9.6 dB and 9.8 dB, respectively.

Most of the noise comes from the G_m cells and the source impedance transformation due to C_s. Increasing the value of C_s lowers the impedance transformation ratio but on the other hand it increases the loading effect of each path on the other one which leads to increase in the loss of the filter. Moreover, it leads to more area consumption (due to the baseband capacitors) and bigger G_m values which indeed increases the noise contribution of the G_m cells. Simulation shows the optimum range for the series capacitor is 1 pF $\leq C_s \leq$ 2 pF. Further increase in C_s leads to excessive loss due to more interaction between the two paths and in contrast reducing the series capacitor increases the NF of the filter considerably. Exploiting $C_s = 2$ pF leads to

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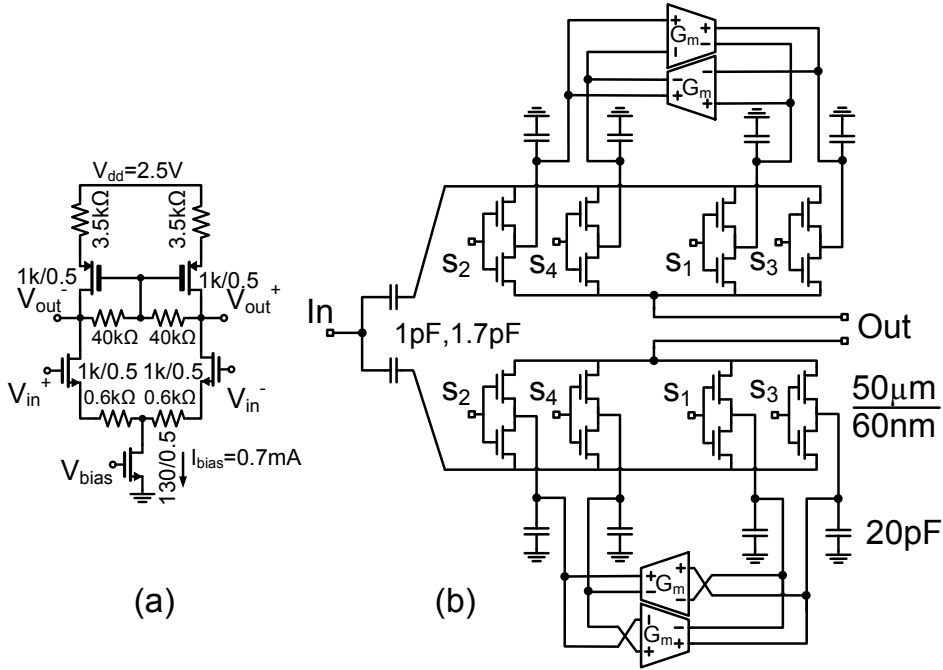
Figure 3.18: (a) Implementation of the differential G_m cells and (b) Schematic of the proposed filter

NF of 8.6 dB and -3.8 dB voltage gain while using $C_s = 1$ pF (our case), leads to NF of 9.8 dB and voltage gain of -2.2 dB. C_s of 1 pF is chosen over 2 pF because of less reduction in the voltage gain of the filter and 50% reduction in the area of the baseband capacitors.

3.5 Realization

The filter was realized in 65 nm CMOS LP technology. The schematic of the proposed filter is illustrated in Fig. 3.18(b). A modulo-4 ring counter has been used to obtain 4 non-overlapping clock signals with 25% duty cycle. The simplified block diagram of the quadrature clock generator with low phase error [108] is shown in Fig. 3.19. A master clock (CLK) at 4 times the switching frequency is applied externally. A D flip-flop based divider divides the input clock by four and produces 4 clock signals with 25% duty cycle. Due to its lower power consumption and higher speed, D flip-flops based on transmission gates have been exploited [108].

Every switch in the filter, which is realized by NMOS transistor, has been sized (W/L $= 50\mu$m/60nm) to obtain an on resistance of 10 Ω. Although the ultimate
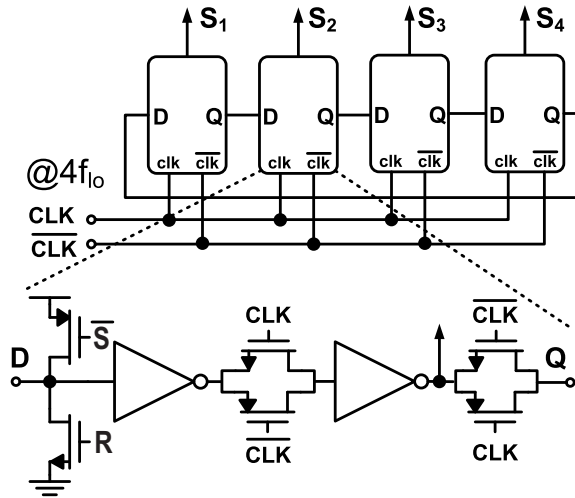
Figure 3.19: A 4-phase non-overlapping clock generator with low phase mismatch (one D flip-flop shown in transistor level)
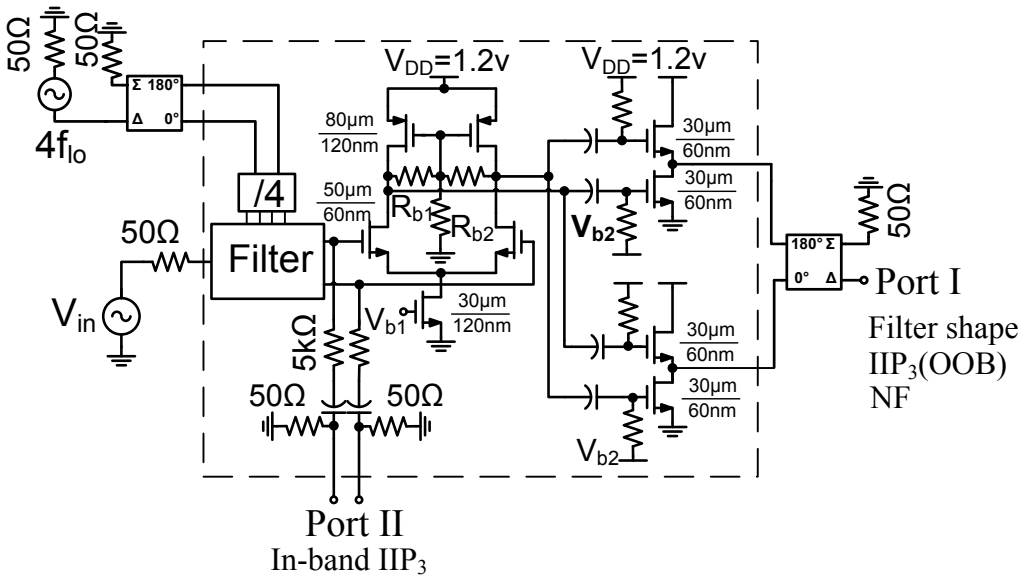
Figure 3.20: Measurement interface
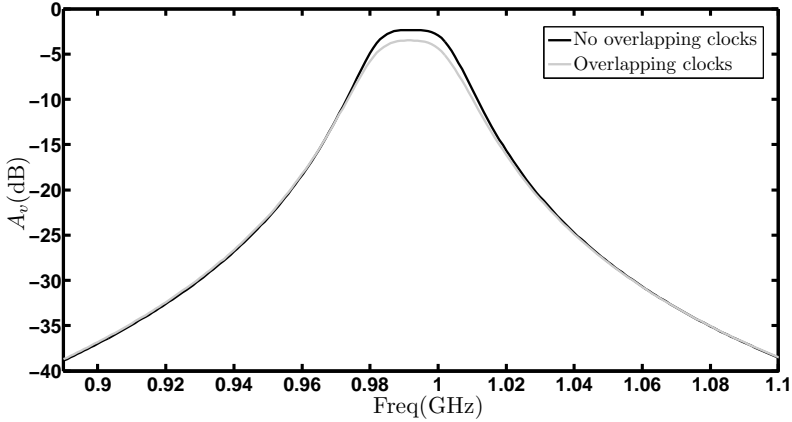
Figure 3.21: The SpectreRF simulation of the transfer function of the filter with and without reducing the cross-points of the adjacent clocks from V$_{\text{DD}}$/2 to lower than V$_{\text{th},n}$

rejection of the filter is relatively independent from the choice of switch resistances, low switch resistances are chosen to reduce their noise and nonlinearity contributions and the mismatch between them. Nevertheless, increasing the size of switches will introduce more parasitic capacitance to the input and output port of the filter which reduces the voltage gain of the filter. In our case, parasitic capacitances introduced 2 dB reduction in the voltage gain of the filter. Moreover, utilization of larger switch transistors increases the dynamic power consumption and the LO leakage to the input port of the filter. Because the drain and source of each switch have a DC bias of 0.8 V, for proper operation (high linearity and low on resistance) of the switches, the low and high levels of the clock signals should be raised by 0.8 V. Simply, the clock signals are ac coupled to the gate of each switch which has a high ohmic resistor to a bias voltage of 1.1 V. The ac-coupling capacitors (MIM capacitors with C = 2 pF) have been sized big enough to minimize the voltage loss due to the capacitive division between the ac-coupling capacitor and gate capacitance of the switches. The overlap between the adjacent clock signals reduces the voltage gain, quality factor and deteriorates the linearity of the filter. The PMOS transistors of inverters in Fig. 3.19 have been weakened compared to NMOS transistors to produce non-overlapping clocks. (The crossing point of adjacent clocks has been lowered from V$_{\text{DD}}$/2 to lower than the threshold voltage of switching transistors.) The transfer function of the filter for adjacent clocks having cross-points of V$_{\text{DD}}$/2 and cross-points lower than V$_{\text{th},n}$ are compared in Fig. 3.21. As can be seen, the overlap between the adjacent clocks introduces about 1 dB reduction in the pass-band gain of the filter. Moreover, overlapping between the adjacent clock signals increases the noise figure by 0.6 dB.

The buffers that drive the switches have been sized to achieve rise and fall time of less than 30 ps. The implementation of the differential G_m cells is depicted in Fig. 3.18(a) which draws 0.7 mA from 2.5 V. Due to the parasitic capacitance of the switches at input RF node which effectively increases the series capacitance, the value of the G_m changed from 0.5 mS to 0.7 mS (G_m cells are slightly tunable). The length of each transistor is chosen to be 0.5 μm to reduce the $1/f$ noise contribution and increase the output impedance. Resistive degeneration has been used to linearize the G_m and lower the $1/f$ noise contribution further. The bias voltage of the input and output of the differential G_m are equal and chosen to be 0.8 V. To obtain a bandwidth of 20 MHz, the baseband capacitors C_{BB} are 20 pF and made from accumulation-mode N-type MOS capacitors which are the densest on-chip capacitors. When they are biased ($V_{GS} > 0$), they are reasonably linear [109]. In our case, each baseband capacitor is biased at 0.8 V. In presence of mismatch among the baseband capacitors and G_m cells of the BPF, any RF input at $f_{lo} + f_m$ can be folded on top of the desired channel as a component at $f_{lo} - f_m$ [104]. The folding is proportional to $\frac{\Delta G_m}{G_m \sqrt{1+(\omega_m/\omega_{BB})^2}} + \frac{\Delta C_{BB}}{C_{BB} \sqrt{1+(\omega_{BB}/\omega_m)^2}}$. The large area of C_{BB} and G_m cells greatly reduces the mismatch between them. Therefore the phase mismatch between the clocks is the dominant factor in reducing the image rejection [106]. Monte-Carlo Simulations show that the folding is < -52 dB for $f_{lo} = 1$ GHz and $f_m = 2$ MHz. Each series capacitor which has two modes is made of two parallel MIM capacitors of 1 pF and 0.7 pF. The selection of the series capacitor value is in this way: for $f_{in} = 0.7 - 1.2$ GHz, C_s is 1 pF and for $f_{in} = 0.4 - 0.7$ GHz, C_s is 1.7 pF. The measurement interface has been illustrated in Fig. 3.20. For NF, filter shape and out of band linearity measurements, two buffer stages have been added after the filter (port I). Moreover, to measure the in-band IIP$_3$ of the filter while not being affected by the non-linearities in the buffers, a simple resistive divider has been used (port II). An ac-coupled differential amplifier is used to perform the subtraction and two push-pull stages are exploited for matching purposes. In the differential amplifier, the gates of the PMOS transistors are connected via a resistor R_{b2} to ground to increase the voltage headroom of the input transistors. In this way, the DC bias of the output voltage of the differential amplifier will be $[1 + R_{b1}/(2R_{b2})] \times (V_{DD} - V_{SGp})$. To maintain the bandwidth and filter shape of the filter over process corners, the value of G_m and C_{BB} should be programmable.[5] Because the center frequency of the filter is set by an external clock frequency, the center frequency of the filter does not change. This is in contrast to G_m-C filters [42] where a separate PLL is needed to correct the center frequency of the filter over process corners.

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[5]In our case, G_m cells are slightly tunable.
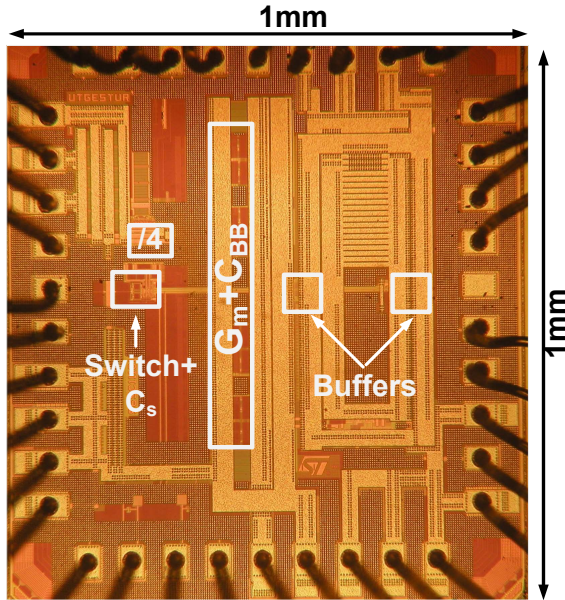
Figure 3.22: 65nm CMOS chip micrograph indicating functional blocks

3.6   Measurements

The chip micrograph of the proposed filter is illustrated in Fig. 3.22. The chip has been fabricated in CMOS LP 65nm technology and the active area of the filter is 0.127 mm^2. The chip is mounted in a QFN24 package and tested on a printed circuit board. The measured transfer function of the filter is compared with the SpectreRF simulation of the proposed filter and a conventional 4-path filter in Fig. 3.23 (with the same baseband capacitor C_{BB} = 20 pF). As can be seen, the ultimate rejection and order of filter have been improved compared to conventional 4-path filters [107]. The tunability of the filter from 0.4 GHz to 1.2 GHz has been measured and illustrated in Fig. 3.24. The measured results are in agreement with the simulation results shown in Fig. 3.14 within 0.3 dB. The maximum pass-band ripple is around 0.4 dB. Although the BPFs at second harmonics of f_{lo} have been suppressed due to subtraction, the BPFs at odd harmonics of the f_{lo} still exist. The voltage gain of the filter at $k f_{lo}$ $k = 3, 5, ...$ is $1/k^2$ times lower than the voltage gain of the filter at f_{lo}. As can be seen in Fig. 3.23, there is almost 20 dB gain difference between the gain of filter at f_{lo} and $3 f_{lo}$. If more filtering is needed, an LTI low-pass filter or harmonic rejection mixer [108] can be utilized. A closer view of the filter shape measurements is illustrated in Fig. 3.25. Because of the constant bandwidth nature of the N-path filters, the
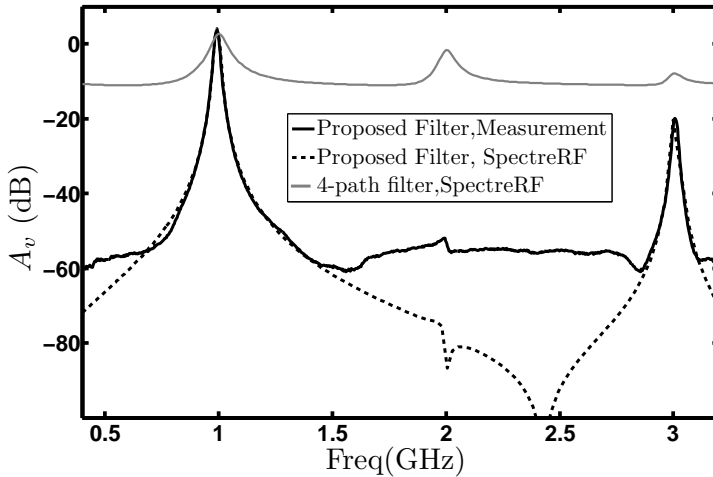
Figure 3.23: Comparing the measured filter shape at 1GHz with the SpectreRF simulation of the proposed filter and conventional 4-path filter (The gain of the buffers is estimated from the SpectreRF simulation and has been de-embedded from the measurement.)

quality factor of the filter reduces as the center frequency of the filter reduces. In our case, the quality factor Q changes from 60 for $f_c = 1.2$ GHz to 20 for $f_c = 0.4$ GHz. In N-path filters, there is a direct trade-off between area (which is consumed by baseband capacitors) and quality factor. Furthermore, the quality factor can be enhanced by increasing the source resistance. The transfer function of 10 samples has been measured to demonstrate the consistency of the filter against mismatch. These measurements are shown in Fig. 3.26. As can be seen, the filter shape is quite robust to the mismatch. The ultimate rejection of the filter is approximately 58 dB which is probably limited by the direct coupling between the input and output bond wires. The measured in-band IIP_3 of the filter is +9 dBm which has been measured at port II in Fig. 3.20 while the simulated in-band IIP_3 is +11 dBm. It is found in simulation that reducing the overlap between the adjacent clock signals (lowering the cross-point of adjacent clocks to lower than the threshold voltage of switching transistors), increases the IIP_3 of the filter by 1.8 dBm. Because of the high linearity of the switches and baseband capacitors, the linearity of the filter is mainly limited with G_m cells. The measured out of band IIP_3 for an offset frequency of $\Delta f = +50$ MHz is +29 dBm which was measured at port I in Fig. 3.20. Due to the large amount of filtering before the buffers, the nonlinearity of the buffers is not important in the measurement of out of band IIP_3. Another measurement has been performed to check the persistency of the filter shape and its ultimate rejection when a large
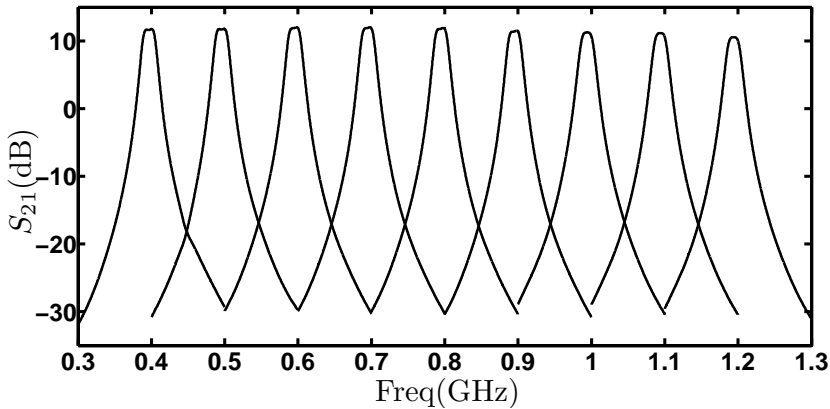
Figure 3.24: Measured transfer function of the filter from 0.4 GHz to 1.2 GHz
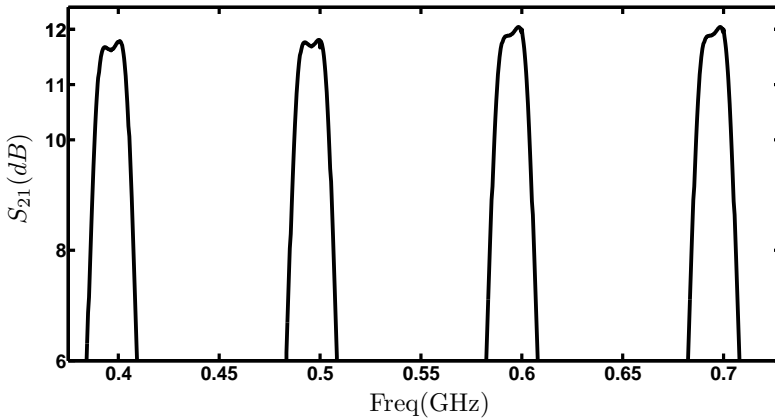
Figure 3.25: Measured passband shape of the filter

out of band interferer exists very near to the passband of the filter. The measured transfer function of the filter with and without a +2 dBm continuous wave blocker which is located at +50 MHz and +30 MHz offset from the center frequency of the filter has been measured and compared in Fig. 3.27 and as can be seen, the filter is quite robust to the large out-of-band interferers. A +2 dBm blocker located at +30 MHz offset from the center frequency of the filter reduces the passband gain by 1.5 dB (at port II in Fig. 3.20). The LO leakage power to the input port of the filter is < -60 dBm which is mainly caused by the capacitive mismatch in the switches. The measured NF of the filter is 10 dB (the noise of buffers is calculated from simulation and de-embedded from the measurement.) which is in agreement with the theory and simulation (Fig. 3.17). Most of the noise comes from G_m cells and the impedance
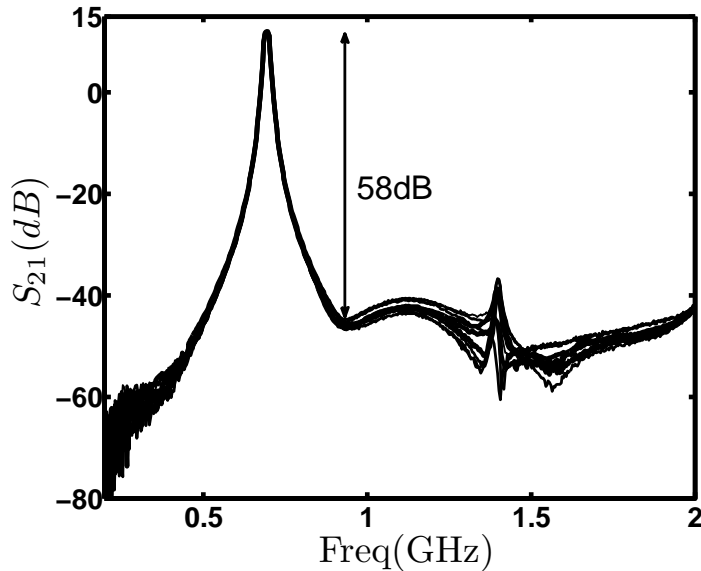
Figure 3.26: Measurements of transfer function of 10 samples to demonstrate the consistency of the filter against mismatch

Table 3.1: Comparison between measurement and simulation results

	Measurement	Simulation
BW [MHz]	21	21
Stopband Rej. [dB]	> 55	> 70
IIP3$_{IB}$ [dBm]	$> +12$	$> +10.6$
IIP3$_{OOB}$ [dBm] ($\Delta f= +50$MHz)	$+29$	$+32$
NF [dB]	$9.7 - 10.5$	$9.6 - 10.3$
Ripple [dB]	< 0.4	< 0.6
Gain [dB]	$-2, -3.2$	$-1.7, -2.7$

transformation of the source resistance due to the series capacitors C_s. A comparison between simulation and measurement has been done in Table 3.1. Furthermore, a comparison between measurements and simulation results of NF and IIP$_3$ over the whole band has been done in Fig. 3.28.

N-path filters for good linearity and low noise figure need clock signals with low rise and fall time to drive large switches which indeed raises the dynamic power consumption of the filter. The static power consumption is 7 mW over the tuning band and the dynamic power consumption varies from 5.8 mW to 14.4 mW. The filter is compared with [19, 20, 97, 103, 107, 110, 111] in Table 3.2. We added filtering-
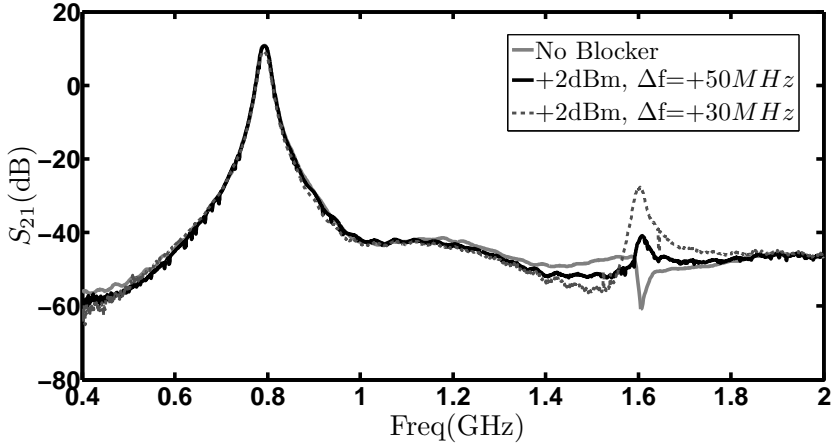
Figure 3.27: The measured transfer function of the filter with and without +2dBm continuous wave blocker which located +50MHz and +30MHz offset far from the center frequency of the filter
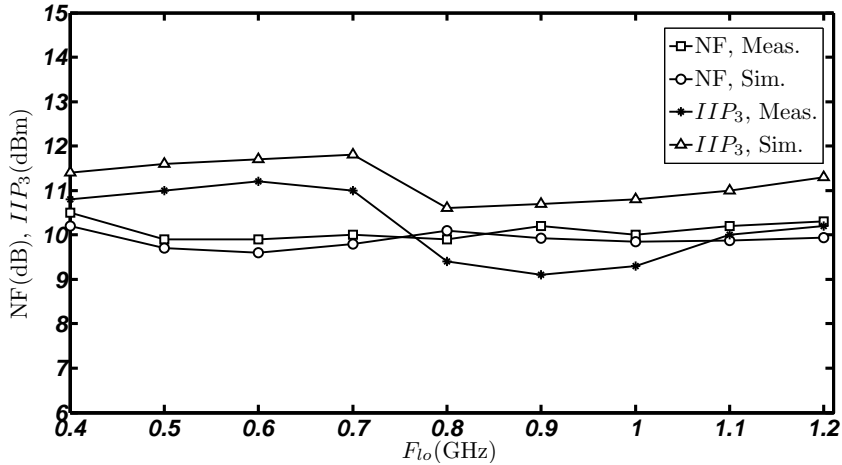
Figure 3.28: The measured and simulated IIP$_3$ and NF of the proposed filter over the whole band

Table 3.2: Comparison Table

	[103]	[19]	[107]	[110]	[20]	[111]	[97]	This work
Type	Receiver		Filter					
Tech.[a][nm]	65	65	65	65	250	SiGe250	350	65
$f_{\text{cen.}}$ [GHz]	2.14	$0.05 - 2.4$	$0.1 - 1$	0.08	2.14	2.14	$0.24 - 0.53$	$0.4 - 1.2$
Order	6	2	2	4	6	4	2	4
BW[MHz]	4	20	35	10	60	60	$2 - 5$	21
Ult.-Rej.[dB]	48	13	16	32	N.A.	28	24	55
IIP3_{in}[dBm]	-8.5	-67	$+19$	-2	-4.9	$+35$	< -40	$+9$
IIP3_{oob}[dBm]	-6.3	$+25$	N.A.	N.A.	N.A.	N.A.	N.A.	$+29$[b]
NF[dB]	5.3	5.5	5.5	21.5	19	9	9	10
Area[mm^2]	0.76	2.5	0.07	0.25	3.51	6.65	1.93	0.127
Ripple[dB]	N.A.	N.A.	N.A.	0.1	0.7	1.5	N.A.	0.4
P_{DC}[mW]	34.2	60	18	13.2	17.5	7	63	21.4

[a] CMOS, unless otherwise stated.
[b] $\Delta f = +50$ MHz.

receivers [19, 103] in the comparison table. Our filter outperforms Q-enhancement [20] and G_m-C [110] filters from a linearity, noise and tunability point of view. According to [14], the DR of G_m-C filters depends on $1/Q^2$ while the dynamic range of Q-enhancement filters depends on Q_0^2/Q^2 where Q_0 is the quality factor of on-chip inductors. G_m-C filters need extra circuitry (gyrators) to synthesize inductors and Q-enhancement filters require extra circuitry (a negative impedance) to enhance the Q of on-chip inductors and these extra circuitries lead to a lower DR. However in the N-path technique, the required Q of the filter can be obtained by increasing C_{BB} ($Q \propto C_{\text{BB}} R_x$) and no extra active devices is needed. Therefore the Q of the N-path filter is decoupled from its DR. The DR [14] of the proposed filter is 95 dB in 1 MHz bandwidth. According to the FOM defined in [14], the FOM of our filter is 146.4 dB-Hz/mW at $f_c = 1$ GHz and 148.5 dB-Hz/mW at $f_c = 0.4$ GHz which is higher than the FOM of the Q-enhancement filters [20] (129.2 dB-Hz/mW) and [21] (125.6 dB-Hz/mW). Compared to [19, 107], it has better pass-band shape and much higher rejection at RF frequencies. Moreover, this work has comparable out of band rejection and better pass band shape compared to [103]. The proposed filter is a good candidate for substituting the SAW filters used in IF section of a Super-Heterodyne receiver where the IF frequency can be adapted to actual interference conditions.

3.7   Conclusions

A 4$^{\text{th}}$ order switched G$_m$-C BPF technique is proposed to improve the filter shape and ultimate rejection of 4-path passive mixer filters. The technique exploits subtraction of output voltages of the two 2$^{\text{nd}}$ order 4-path bandpass filters with shifted center frequency. The frequency shift of the 4-path BPF is realized by coupling the baseband capacitor voltages via two differential transconductors, in either a clockwise or counter clockwise fashion. Capacitive splitting of the input signal is used to reduce mutual loading of the two 4-path BPFs and increase their quality factors. The center frequency of the filter is tunable form 0.4 GHz to 1.2 GHz with a bandwidth of around 21 MHz. The ultimate rejection of the filter is > 55 dB and the in-band and out of band (Δf = +50 MHz) IIP$_3$ of the filter are +9 dBm and +29 dBm, respectively. The NF of the filter is 10 dB. The filter NF is similar to a typical mixer NF and therefore it is not suitable for antenna filter applications. Typically in fully integrated receivers, filtering is needed at different places along the receiver chain where our proposed filter can perform some of the required filtering, especially where tunability and integration are important. This filter is a good candidate for substituting the SAW filters used in IF section of a super-heterodyne receiver where the IF frequency can be adapted to actual interference conditions. Moreover, because the impedance level of an IF section is typically much higher than 50 Ω, the quality factor of the filter can be increased considerably compared to the case where R$_s$ is 50 Ω. The power consumption of the filter varies from 12.8 mW to 21.4 mW over the tuning frequency range. The filter has been fabricated in CMOS LP 65 nm technology and the active area is 0.127 mm^2.

3.A   An N-path Filter with Generic Source and Baseband Impedances

Firstly, the transfer function of an N-path filter with a generic source admittance and a generic but with limited bandwidth baseband admittance will be calculated. This formulas are used in the body of this chapter to analyze the effect of the added G$_m$ cells on a conventional 4-path filter. Moreover based on these calculations, the effects of the addition of a series capacitor to the source resistance of a conventional 4-path filter on its transfer function and NF will be analyzed. Finally, the NF of the final filter shown in Fig. 3.11 will be calculated.

With a derivation analogous to [83, 101] and by assuming that: 1) N is the number of phases and the duty cycle of the clock signals $s_i(t)$ ($i = 1 - \text{N}$) is 1/N, 2) ω_{lo} is the switching frequency, 3) Y$_s$=Y$'_s$/$\left(\text{R}_{sw}\text{Y}'_s + 1\right)$, 4) If there is an interaction between the baseband nodes (like the g_ms in our case), the effective baseband admittance Y$_{\text{BB}}(s, k)$ will be different for f_{in} around $k f_{\text{lo}}$ $k \in \mathbb{Z}$ 5) To take into account the

effect of the harmonics of f_{lo} , we define an effective source admittance[6] $Y_{s,\text{eff},k}(s)$ for f_{in} around kf_{lo} $k \in \mathbb{Z}$ 6) $a_m = \frac{e^{-j\pi m/N}}{N} \times \text{sinc}\,(\pi m/N)$ is the Fourier coefficient of $s_1(t)$, and 7) Each switch is modeled with an ideal switch in series with switch resistance R_{sw} and parasitic capacitance of the switches is not taken into account, the total transfer function of an N-path filter with a generic source admittance and a generic but with limited bandwidth baseband admittance (Fig. 3.29) can be written in the form of:

$$V_x(s) = \sum_{l=-\infty}^{+\infty} H_l(s) \times V_{\text{in}}(s - jlN\omega_{\text{lo}})$$

$$H_l(s) = \sum_{m=-\infty}^{+\infty} N^2 a_m a_{lN-m} Z_x(s - jm\omega_{\text{lo}}, k) \times Y_s(s - jlN\omega_{\text{lo}})$$

(3.11)

where l is a folding back index term and $Z_x(s, k)$ is described by:

$$Z_x(s, k) = \frac{1}{NY_{\text{BB}}(s, k) + Y_{s,\text{eff},k}(s)}$$

$$Y_{s,\text{eff},k}(s) = \sum_{m=-\infty}^{+\infty} N^2 |a_{Nm-k}|^2 Y_s(s - j\omega_{\text{lo}}(Nm - k))$$

(3.12)

To find the transfer function of the filter with no net frequency translation, the l in (3.11) should be zero. Consequently, $V_x(s)/V_{in}(s)$ will be:

$$T(s) = \frac{V_x(s)}{V_{\text{in}}(s)} = Y_s(s) \times \sum_{m=-\infty}^{+\infty} \text{sinc}^2\,(m\pi/N)\,Z_x(s - jm\omega_{\text{lo}}, m) \tag{3.13}$$

$V_{\text{out}}(s)/V_{\text{in}}(s)$ can be found using superposition and substitution theorem and it will be $\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{T(s) + R_{sw}Y'_s(s)}{R_{sw}Y'_s(s) + 1}$. Furthermore, (3.11) can be exploited to find the folding back components from $\omega_{\text{in}} = (1 - mN)\omega_{\text{lo}} + \Delta\omega$ to $\omega_{\text{out}} = \omega_{\text{lo}} + \Delta\omega$, $m \in \mathbb{Z}$ (3.14).

$$A_{\text{fold}}|_{\omega_{\text{lo}}+\Delta\omega} = \text{sinc}^2\,(\pi/N) \times \frac{1}{mN - 1} \times Z_x(\Delta\omega, 1 - mN) \times Y_s((1 - mN)\omega_{\text{lo}} + \Delta\omega)$$

(3.14)

In the case of a resistive source admittance $Y'_s = 1/R_s$, the effective admittance of $Y_{s,\text{eff},k}$ is simplified to $1/(R_s + R_{sw})$. Therefore, (3.13) will be simplified to (3.15).

---

[6]In the case of $Y'_s = 1/R_s$, the effective source admittance will be $1/(R_s + R_{sw})$.
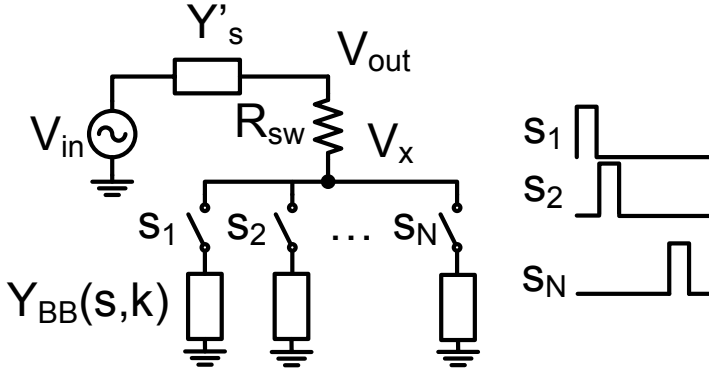
Figure 3.29: An N-path Filter with generic source admittance and generic but limited bandwidth baseband admittance exploiting non-overlapping clock signals

$$\mathrm{T}(s) = \frac{\mathrm{V}_x(s)}{\mathrm{V}_{\mathrm{in}}(s)} = \sum_{k=-\infty}^{+\infty} \mathrm{sinc}^2\left(\frac{k\pi}{\mathrm{N}}\right) \times \mathrm{G}(s - jk\omega_{\mathrm{lo}}, k) \qquad (3.15)$$

Where $G(s, k)$ is a LPF due to the combination of a baseband admittance $Y_{BB}(s, k)$ and a source resistance and described in[7] (3.16).

$$\mathrm{G}(s, k) = \frac{1}{(\mathrm{R}_s + \mathrm{R}_{sw})\mathrm{N}\mathrm{Y}_{\mathrm{BB}}(s, k) + 1}, \quad f_{\mathrm{in}} \text{ around } kf_{\mathrm{lo}} \ k \in \mathbb{Z} \qquad (3.16)$$

3.B Addition of a Series Capacitor to the Source Impedance of a 4-path Filter

Now based on (3.12-3.14), the effects of a series capacitor with the source resistance (Fig. 3.30) on the transfer function of a 4-path filter can be investigated. In our case, $\mathrm{N} = 4$ and $Y_s(s) = 1/\mathrm{R}_x \times \tau_s s/(1 + \tau_s s)$ where $\tau_s = \mathrm{R}_x \times \mathrm{C}_s$ and $\mathrm{R}_x = \mathrm{R}_s + \mathrm{R}_{sw}$. By using (3.13), the transfer function of the filter around f_{lo} can be found. Therefore due to the limited bandwidth of the baseband admittances, only the two terms ($m = 1, -1$) of (3.13) are of interest.

$$\mathrm{T}(s) = \frac{\mathrm{V}_x}{\mathrm{V}_{\mathrm{in}}} = \frac{8}{\pi^2 \mathrm{R}_x} \times \frac{\tau_s s}{1 + \tau_s s} \times (\mathrm{Z}_x(s - j\omega_{\mathrm{lo}}, 1) + \mathrm{Z}_x(s + j\omega_{\mathrm{lo}}, -1)) \qquad (3.17)$$

---

[7]Because each baseband admittance sees $R_s + R_{sw}$ for $1/N^{th}$ of the clock period, the effective resistance that each baseband admittance sees is $\mathrm{N}(R_s + R_{sw})$
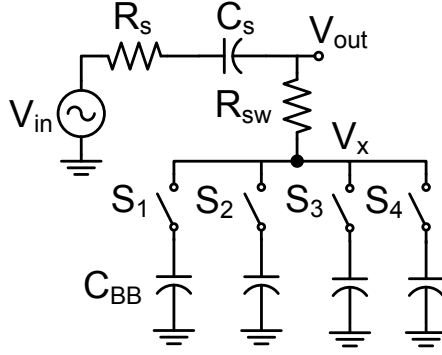
Figure 3.30: Addition of a series capacitor C_s to the source resistance R_s of a conventional 4-path filter

$Z_x(s, \pm 1)$ is found using (3.12).

$$Z_x(s, \pm 1) = \frac{1}{4C_{BB}s + j\text{Imag}(Y_{s,\text{eff},\pm 1}) + \text{Real}(Y_{s,\text{eff},\pm 1})} \tag{3.18}$$

From (3.12), the effective source admittance $Y_{s,\text{eff},1}$ for input frequencies around f_{lo} by assuming that $|\omega| << |(4m - 1)\omega_{\text{lo}}|$ $(m \in \mathbb{Z})$ can be found.

$$Y_{s,\text{eff},1} \cong \sum_{m=-\infty}^{+\infty} 16|a_{4m-1}|^2 Y_s(-j\omega_{\text{lo}}(4m - 1))$$

$$\cong \frac{8}{\pi^2 R_x} \times \sum_{m=-\infty}^{+\infty} \frac{1}{(4m - 1)^2} \times \frac{-j\tau_s\omega_{\text{lo}}(4m - 1)}{1 - j\tau_s\omega_{\text{lo}}(4m - 1)} \tag{3.19}$$

It can be proven that $\text{Imag}(Y_{s,\text{eff},-1}) = -\text{Imag}(Y_{s,\text{eff},1})$ and $\text{Real}(Y_{s,\text{eff},-1}) = \text{Real}(Y_{s,\text{eff},1})$. The real and imaginary parts of $Y_{s,\text{eff},1}$ in terms of R_x and $\tau_s\omega_{\text{lo}}$ have been illustrated in Fig. 3.31. Interestingly as can be seen from Fig. 3.31, for $\tau_s\omega_{\text{lo}} < 0.5$, both real and imaginary parts of the $Y_{s,\text{eff},1}$ can be well estimated by $2\tau_s\omega_{\text{lo}}/(\pi R_x)$. Therefore by utilizing the mentioned approximation, (3.17) can be changed to:

$$T(s) \cong \frac{V_x}{V_{\text{in}}} = \frac{8}{\pi^2} \times \frac{\tau_s s}{1 + \tau_s s} \times \frac{s/(2R_x C_{BB})}{s^2 + (C_s\omega_{\text{lo}}/(\pi C_{BB}))s + \omega_{\text{lo}}^2 \times (1 - C_s/(\pi C_{BB}))} \tag{3.20}$$

Now, the effect of a series capacitor with source resistance on the noise figure of a conventional 4-path filter will be investigated. By using (3.14), the output noise voltage at node V_x can be found.
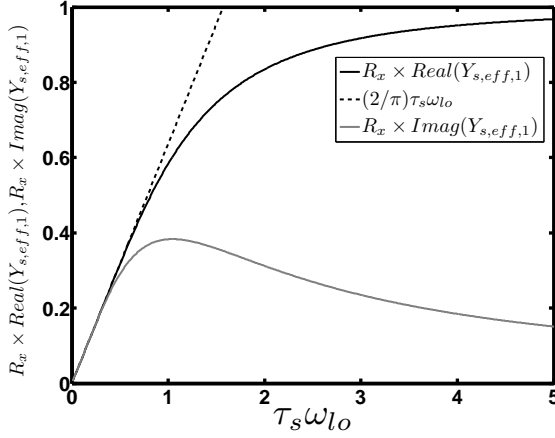
Figure 3.31: $\mathrm{R}_x \times \mathrm{Imag}(\mathrm{Y}_{s,\mathrm{eff},1})$, $\mathrm{R}_x \times \mathrm{Real}(\mathrm{Y}_{s,\mathrm{eff},1})$ and their approximation as a function of $\tau_s\omega_{\mathrm{lo}}$

$$\overline{\mathrm{V}^2_{x,n_{\omega_{\mathrm{lo}}+\Delta\omega}}} = 4k\mathrm{TR}_x \sum_{m=-\infty}^{+\infty} \mathrm{A}^2_{\mathrm{fold}} = 4k\mathrm{TR}_x \times \frac{64(\tau_s\omega_{\mathrm{lo}})^2}{\mathrm{R}^2_x\pi^4} \times \sum_{m=-\infty}^{+\infty} \frac{|\mathrm{Z}_x(\Delta\omega, 1-4m)|^2}{1+\tau_s^2\omega_{\mathrm{lo}}^2(1-4m)^2} \tag{3.21}$$

It can be proven that $\mathrm{Z}_x(s, 1-4m) = \mathrm{Z}_x(s, 1)$. (3.21) can be simplified for $\tau_s\omega_{lo} < 0.5$ using Fig. 3.31.

$$\overline{\mathrm{V}^2_{x,n_{\omega_{\mathrm{lo}}+\Delta\omega}}} \cong 4k\mathrm{T} \times \frac{16\tau_s\omega_{lo}}{\mathrm{R}_x\pi^3} \times |\mathrm{Z}_x(\Delta\omega, 1)|^2 \tag{3.22}$$

By exploiting (3.17), the gain of the 4-path filter with a series capacitor around f_{lo} is $\frac{8}{\pi^2\mathrm{R}_x} \times \frac{j\tau_s\omega}{1+j\tau_s\omega} \times \mathrm{Z}_x(\Delta\omega, 1)$. Consequently, the NF at node V_x is described in (3.23).

$$\mathrm{F}|_{\omega=\omega_{\mathrm{lo}}+\Delta\omega} \cong \left(1 + \frac{\mathrm{R}_{sw}}{\mathrm{R}_s}\right) \times \frac{\pi}{4} \times \left(\omega_{\mathrm{lo}}\tau_s + \frac{1}{\tau_s\omega_{\mathrm{lo}}} \times \left(\frac{\omega_{\mathrm{lo}}}{\omega}\right)^2\right) \tag{3.23}$$

3.C   NF Calculation of the Implemented Filter

In this section we develop the material needed to derive the NF of the resultant filter shown in Fig. 3.11. The total output noise voltage of the filter shown in Fig. 3.11 for $\omega_{\mathrm{lo}}\tau_s < 0.5$ (excluding the noise contribution of the differential G$_m$ cells and

neglecting the mutual loading effect of each path on the other one) is found in a similar way as (3.21).

$$\overline{V_{out,n}^2} \cong 8k\mathrm{TR}_{sw} + 4k\mathrm{T} \times \frac{16\mathrm{C}_s\omega_{lo}}{\pi^3} \times \left(|Z_{x,\mathrm{path1}}(s,1)|^2 + |Z_{x,\mathrm{path2}}(s,1)|^2\right) \quad (3.24)$$

Where $Z_{x,\mathrm{path1}}(s,1)$ and $Z_{x,\mathrm{path2}}(s,1)$ are:

$$
\begin{aligned}
Z_{x,\mathrm{path1}}(s,1) &= \frac{1}{4\mathrm{C}_{\mathrm{BB}}(s - j\omega_{\mathrm{BB}}) + \frac{2}{\pi}\mathrm{C}_s\omega_{lo}(1+j)} \\
Z_{x,\mathrm{path2}}(s,1) &= \frac{1}{4\mathrm{C}_{\mathrm{BB}}(s + j\omega_{\mathrm{BB}}) + \frac{2}{\pi}\mathrm{C}_s\omega_{lo}(1+j)}
\end{aligned}
\quad (3.25)
$$

and ω_{BB} is $g_m/\mathrm{C}_{\mathrm{BB}}$. Note that the first term in (3.24) is due to the noise contribution of the switch resistances of the second set of switches. In fact, the noise of the switch resistances of the second set of switches is not subject to folding back issues and only the noise contents around f_{lo} will deteriorate the NF. Now, we will investigate the noise contribution of the differential G_m cells. At first, the transimpedance of $\mathrm{V}_{out1}(\omega_{lo}+\Delta\omega)/\mathrm{I}_{n1,2}(\Delta\omega)$ shown in Fig. 3.16(a) will be found. Due to the differential G_m cells and the differential stimulation of the circuit (I_{n1} or I_{n2}), $\mathrm{V}_{b1} = -\mathrm{V}_{b3}$ and $\mathrm{V}_{b2} = -\mathrm{V}_{b4}$. By assuming that $\mathrm{I}_{n2} = 0$ and writing the KCL at nodes V_{b1} and V_{b2}, $\mathrm{V}_{bi}/\mathrm{I}_{ni}$ $i = 1,2$ can be found by assuming that $\tau_s\omega_{lo} < 0.5$ (3.26).

$$
\begin{aligned}
\frac{\mathrm{V}_{b1}(s)}{\mathrm{I}_{n1}(s)} &= \frac{\mathrm{C}_{\mathrm{BB}}s + \frac{1}{2\pi}\mathrm{C}_s\omega_{lo}}{\left(\mathrm{C}_{\mathrm{BB}}s + \frac{1}{2\pi}\mathrm{C}_s\omega_{lo}\right)^2 + 4\left(\mathrm{G}_m - \frac{1}{4\pi}\mathrm{C}_s\omega_{lo}\right)^2} \\
\frac{\mathrm{V}_{b2}(s)}{\mathrm{V}_{b1}(s)} &= \frac{-2(\mathrm{G}_m - \frac{1}{4\pi}\mathrm{C}_s\omega_{lo})}{\mathrm{C}_{\mathrm{BB}}s + \frac{1}{2\pi}\mathrm{C}_s\omega_{lo}}
\end{aligned}
\quad (3.26)
$$

By exploiting $v_{out1}(t) = v_{b1}(t) \times (s_1(t) - s_3(t)) + v_{b2}(t) \times (s_2(t) - s_4(t))$ and the fact that we are just interested in $\mathrm{V}_{out1}(\omega_{lo} + \Delta\omega)$, $\mathrm{V}_{out1}(\omega_{lo} + \Delta\omega)/\mathrm{I}_{n1}(\Delta\omega)$ will be calculated.

$$\frac{\mathrm{V}_{out1}(s + j\omega_{lo})}{\mathrm{I}_{n1}(s)} = 2a_1 \frac{\mathrm{C}_{\mathrm{BB}}s + 2j\mathrm{G}_m + \frac{1}{2\pi}\mathrm{C}_s\omega_{lo} \times (1-j)}{\left(\mathrm{C}_{\mathrm{BB}}s + \frac{1}{2\pi}\mathrm{C}_s\omega_{lo}\right)^2 + 4\left(\mathrm{G}_m - \frac{1}{4\pi}\mathrm{C}_s\omega_{lo}\right)^2} \quad (3.27)$$

Interestingly, $\mathrm{V}_{out1}(s + j\omega_{lo})/\mathrm{I}_{n2}(s)$ will be :

$$\frac{\mathrm{V}_{out1}(s + j\omega_{lo})}{\mathrm{I}_{n2}(s)} = -j \times \frac{\mathrm{V}_{out1}(s + j\omega_{lo})}{\mathrm{I}_{n1}(s)} \quad (3.28)$$

To find the same transfer function for the filter shown in Fig. 3.16(b), it is just needed to change G_m to $-\mathrm{G}_m$ in (3.27) and (3.28). Consequently, the total NF of the

filter will be $F = F_1 + NEF_2$ where F_1 (3.29) is the noise figure of the filter without considering the noise contribution of the G_m cells and NEF_2 (3.30) is the noise excess factor due to the differential G_m cells in both paths.

$$
\begin{aligned}
F_1|_{\omega=\omega_{\text{lo}}+\Delta\omega} = {} & \frac{2R_{sw}}{R_s|T(j\omega)|^2} + \frac{16C_s\omega_{\text{lo}}}{R_s\pi^3|T(j\omega)|^2} \\
& \times \left(|Z_{x,\text{path1}}(\Delta\omega, 1)|^2 + |Z_{x,\text{path2}}(\Delta\omega, 1)|^2\right)
\end{aligned}
\tag{3.29}
$$

$$
NEF_2|_{\omega=\omega_{\text{lo}}+\Delta\omega} = \frac{|I_{nb}|^2}{2kTR_s|T(j\omega)|^2} \times \left(\left|\frac{V_{\text{out1}}}{I_{nb}}\right|^2 + \left|\frac{V_{\text{out2}}}{I_{nb}}\right|^2\right)
\tag{3.30}
$$

Chapter 4

Design of Active N-path Filters

4.1 Introduction

A simple yet effective way to enhance the linearity of a receiver is to eliminate the LNA from receiver chain. In this manner, mixer-first receivers [18, 19] achieve an excellent linearity but at the cost of degradation in NF (Fig. 4.1(a)). It should be noted that due to $1/f$ noise issues, mixer-first receivers are not friendly with process scaling. Of course, it is possible to use an LNA to improve the sensitivity of the receiver but at the cost of degradation in out-of-band linearity (Fig. 4.1(b)).

In this chapter, a widely-tunable and highly-selective filter based on N-path tech-
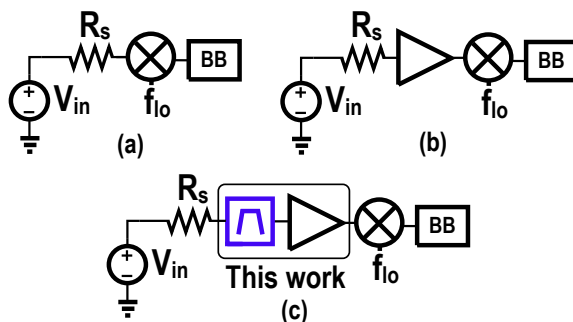
Figure 4.1: (a) A mixer-first receiver (b) Addition of an LNA to improve the sensitivity of the receiver but at the cost of degradation in linearity (c) Proposed work: a highly-selective integrated filter based on N-path technique with an embedded amplification.

nique with a decent amount of embedded amplification is introduced. In this way, while the blockers are eliminated by filtering, the passband gain of the filter relaxes the noise requirement of the following stages in the receiver (Fig. 4.1(c)) [100]. Although , as mentioned in chapter 2, conventional N-path filters provide us with tunable high Q-factor BPFs, they suffer from: 1) harmonic folding; 2) limited stop-band rejection due to the switch resistance, typically 15 dB; and 3) poor filter shape. It is desirable to increase the number of phases in the filter yo reduce the folding-back issues. However, there are trade-offs among the maximum achievable frequency, folding-back issues and the dynamic power consumption. The limited stop-band rejection and poor filter shape issues were tackled in chapter 3 [98, 99]. Exploitation of a second set of switches fundamentally eliminates the effect of switch resistance on the ultimate rejection of the filter at the cost of doubling the dynamic power consumption and the additional noise of the second set of switches (chapter 3). Moreover in chapter 3, a novel method has been utilized to increase the order of the filter and obtain a flat passband shape. However, because the G_m cells in this filter architecture are used in baseband, the $1/f$ noise of the G_ms is upconverted to the center frequency of the filter. Therefore, the size of the baseband transistors should be quite large and lots of resistive degeneration is required to lower the NF of the filter. In this chapter, we propose a filter architecture where the G_m cells are operating around the center frequency of the filter and therefore their $1/f$ noise performance is not critical and minimum channel length transistors can be utilized in the design of the G_m cells, easing process scaling.

Here, we will describe the design methodology and filter properties, especially its transfer function and noise figure. Furthermore, practically achieved results are compared with theory and simulation. The outline of this chapter is as follows: In section 4.2, the proposed idea of an active N-path filter is illustrated and the design methodology is introduced. Moreover, a simple method to calculate the transfer function of conventional N-path filters is shown. In section 4.3, the design of a sixth-order BPF based on the proposed concept is demonstrated. In section 4.4, we will show the realization and simulation results and in section 4.5, the measurement results will be shown. In the last section, conclusions will be drawn.

4.2   High-order Active N-path Filters

An N-path filter can emulate an LC tank with a tunable center frequency and constant bandwidth [19, 98, 103]. Therefore, we conjecture that it should be possible to exploit this property to synthesize high-order BPFs. A singly-terminated 6th order LC BPF is illustrated in Fig. 4.2(a). Parallel LC tanks can be replaced by their N-path counterparts. Therefore, it is required to synthesize the series LC tank from a parallel
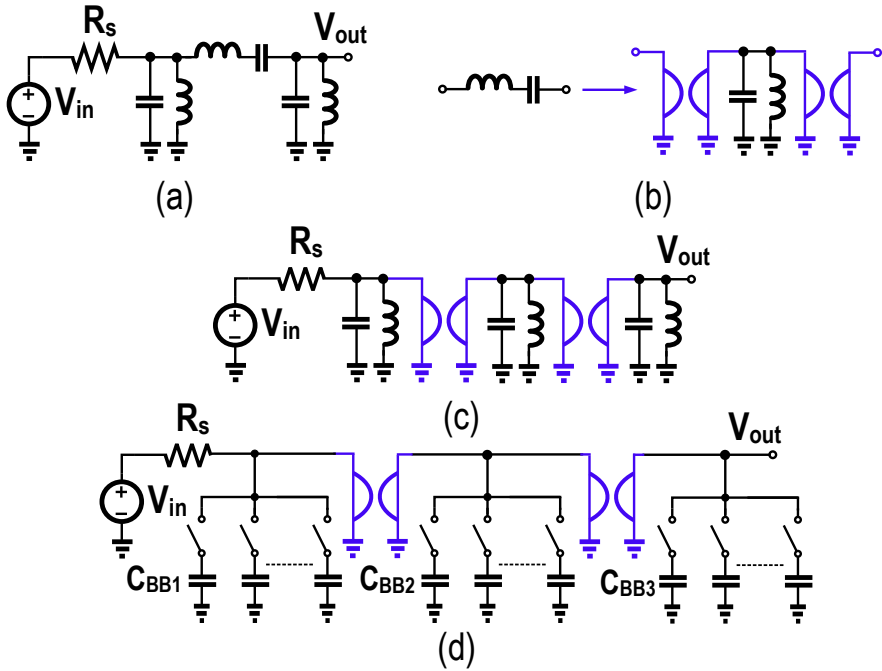
Figure 4.2: (a) A 6th-order singly terminated LC BPF (b) Using two gyrators to synthesize a series LC tank by a parallel one (c) Substitution of the series LC tank by a parallel one (d) Substitution of all parallel LC tanks by their switched capacitor counterparts.

one. The series LC tank can be synthesized using two gyrators as illustrated in Fig. 4.2(b). By substituting the series LC tank in Fig. 4.2(a) with its counterpart in Fig. 4.2(b), the filter shown in Fig. 4.2(c) will result. Now, we substitute each LC tank in the filter by its N-path counterpart and the filter is modified to the filter illustrated in Fig. 4.2(d). The analysis of the filter in Fig. 4.2(d) can become quite complex. In the following sections we will introduce a compact way to analyze N-path filters and design higher order active N-path filters. This provides both an analysis of the filter in Fig. 4.2(d), as well as a general design methodology starting with baseband filters that arrives at the same topology as Fig. 4.2(d).

4.2.1   Compact Analysis of Conventional N-path filters

Here, the transfer function of an N-path filter around its switching frequency is analyzed in an intuitive way, simpler than the methods used in [103, 106] where exhaustive analysis has been utilized. A conventional N-path filter with its required clock signals
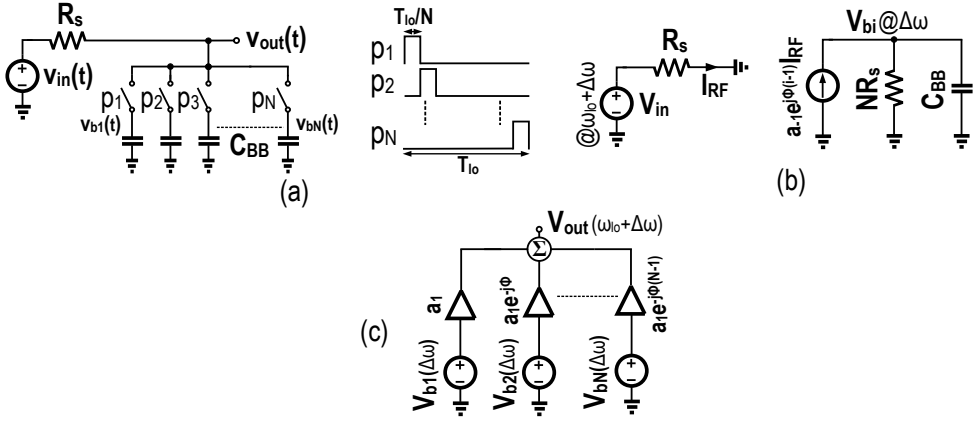
Figure 4.3: (a) A general N-path filter with its required non-overlapping clocks (b) A circuit to simplify the calculation of the baseband voltages, V_{bi}, of the N-path filter and (c) Baseband signals, V_{bi} are upconverted to around ω_{lo} at node V_{out} due to the mixing operation of switches.

is depicted in Fig. 4.3(a). The clock signals, $p_i(t)$ $i = [1, N]$, are non-overlapping with a duty-cycle of 1/N. It is assumed that $R_s C_{BB} \gg T_{lo}$ [83] which means that the baseband voltages in Fig. 4.3(a), V_{bi} $i = [1, N]$, only contain low frequency (baseband) signals. For the time that $p_i(t)$ is high, the current through the source resistance is $[v_{in}(t) - v_{bi}(t)] / R_s$. This can be regarded as the superposition of two currents: an RF current that is caused by $v_{in}(t)$, and a baseband current caused by $v_{bi}(t)$. This allows us to find the baseband voltage of one path, V_{bi}, with the help of the equivalent circuit in Fig. 4.3(b) where the left part works at RF and the right part works at baseband. Firstly, the RF current, $v_{in}(t)/R_s$, will be converted to a baseband current due to the mixing operation of $p_i(t)$. Let us assume that the input signal is located at $\omega_{lo} + \Delta\omega$, $v_{in}(t) = V_{in}e^{j(\omega_{lo}+\Delta\omega)t}$. In this way, the magnitude of the effective baseband current that goes to the baseband capacitor due to the input voltage is $a_{-1}e^{j\phi(i-1)}V_{in}/R_s$ where $a_{-1}e^{j\phi(i-1)}$ is the first Fourier coefficient of $p_i(t)$ and ϕ is the phase difference between $p_1(t)$ and $p_2(t)$. Secondly, the baseband current $-V_{bi}/R_s$ is only present for $1/N^{th}$ of the time, so its effect on the baseband voltage V_{bi} can be modeled by a shunt resistance of NR_s. Therefore, $V_{bi}(\Delta\omega)$ as a function of input voltage, $V_{in}(\omega_{lo} + \Delta\omega)$, will be:

$$V_{bi}(\Delta\omega) = a_{-1}e^{j\phi(i-1)}I_{RF} \times \frac{NR_s}{jNR_sC_{BB}\Delta\omega + 1} = Na_{-1}e^{j\phi(i-1)}G(\Delta\omega)V_{in}(\omega_{lo} + \Delta\omega),$$

(4.1)
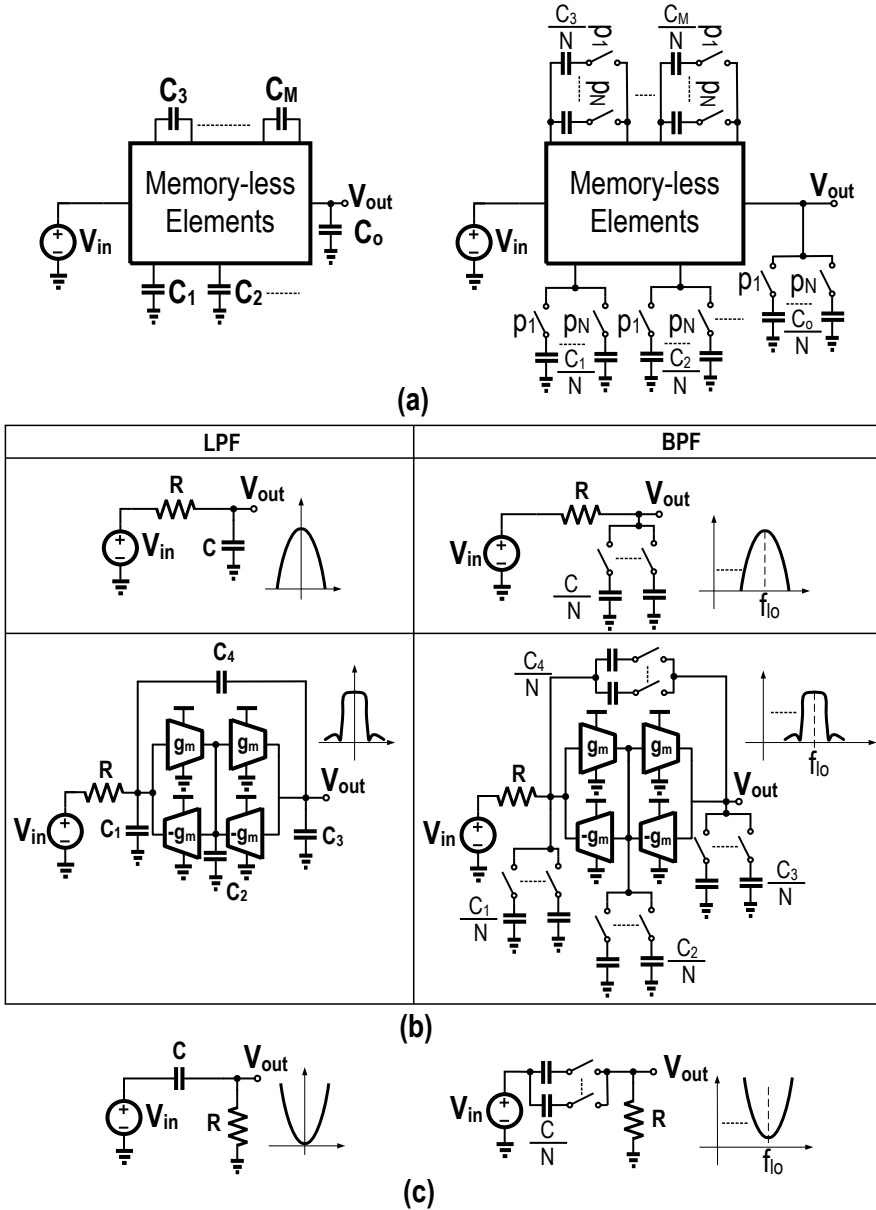
Figure 4.4: (a) Illustration of the design methodology (b) Two examples of exploitation of the methodology (c) A case [112] where the methodology should be utilized indirectly.

where G($\Delta\omega$) is

$$G(\Delta\omega) = \frac{1}{j\mathrm{N}\mathrm{R}_s\mathrm{C}_{\mathrm{BB}}\Delta\omega + 1}. \tag{4.2}$$

Next, we calculate the effect of the baseband voltages on $\mathrm{V}_{\mathrm{out}}$. Due to the transparency of the switches, the voltage of all the baseband nodes, V_{bi}, are upconverted from $\Delta\omega$ to around $\omega_{\mathrm{lo}} + \Delta\omega$ at node $\mathrm{V}_{\mathrm{out}}$ by the mixing operation of the clock signals. As shown in Fig. 4.3(c), the contribution of each path to the output node is $\mathrm{V}_{bi}a_1 e^{-j\phi(i-1)}$ which can be simplified to $\mathrm{N}|a_1|^2\mathrm{G}(\Delta\omega)\mathrm{V}_{\mathrm{in}}(\omega_{\mathrm{lo}} + \Delta\omega)$ using (4.1). These signals are added together to construct the output voltage as illustrated in Fig. 4.3(c). Interestingly, the contribution of all the paths are identical and therefore the output voltage $\mathrm{V}_{\mathrm{out}}(\omega_{\mathrm{lo}} + \Delta\omega)$ will be N times the contribution of one path as described in (4.3).

$$\frac{\mathrm{V}_{\mathrm{out}}(\omega_{\mathrm{lo}} + \Delta\omega)}{\mathrm{V}_{\mathrm{in}}(\omega_{\mathrm{lo}} + \Delta\omega)} = \mathrm{N}^2|a_1|^2\mathrm{G}(\Delta\omega) = \mathrm{sinc}^2\left(\frac{\pi}{\mathrm{N}}\right)\mathrm{G}(\Delta\omega) \tag{4.3}$$

The transfer function described in (5.4) is the transfer function of the N-path filter when the switched-capacitor section is substituted by a capacitor of $\mathrm{NC}_{\mathrm{BB}}$. Therefore in general, to find the transfer function of the filter: 1) substitute the switches and capacitors with a baseband equivalent capacitor of $\mathrm{NC}_{\mathrm{BB}}$; 2) calculate the transfer function of the filter, $\mathrm{G}(s)$; 3) transform this transfer function to around ω_{lo} and 4) multiply the resultant transfer function by $\mathrm{sinc}^2(\pi/\mathrm{N})$. Interestingly, in N-path filters, the bandwidth and center frequency of the filter can be chosen independently. The bandwidth (Hz) of the filter is $1/(\mathrm{N}\pi\mathrm{R}_s\mathrm{C}_{\mathrm{BB}})$ and the Q-factor of the filter is $f_{\mathrm{lo}}\mathrm{N}\pi\mathrm{R}_s\mathrm{C}_{\mathrm{BB}}$.

4.2.2 Design Methodology of Higher Order N-path Filters

In order to calculate the transfer function of a general active N-path filter, we need to make two observations: 1) the transfer function of LPTV (Linear Periodic Time Variant) circuits is the same at all the harmonics of the clock frequency (including the zeroth harmonic) except with a different scaling factor [83, 88, 92, 93, 94].[1] Therefore it is only needed to find the frequency response of the filter at low frequency and the transfer function of the filter around f_{lo}, will be a scaled version of that filter shape, $\mathrm{sinc}^2(\pi/\mathrm{N})$, transformed to f_{lo}, similar to the case described in subsection 4.2.1. This holds only when the output node of the LPTV circuit is band-limited. If the circuit is not band-limited, it is not possible to neglect the contributions at f_{lo} caused by the filter transfer functions around higher harmonics of f_{lo}; 2) at very low frequencies,

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[1]If there is an interaction between the different phases of the N-path filter (e.g. [98]), the transfer function of the filter will not look the same at different harmonics of f_{lo}.

the phase difference between different paths of the filter is zero. Therefore the steady-state voltage on different capacitors of one N-path section would be the same and as a consequence, to find the transfer function of the filter, all the capacitors of one section can be connected together. Therefore, to find the transfer function of a general N-path filter at very low frequency, we substitute each switched-capacitor section of the filter with N times the baseband capacitor of that section and then calculate the transfer function of the resultant circuit. Afterwards, the transfer function of the filter around f_{lo}, is this transfer function which is transformed to around f_{lo} and scaled by scaling factor, $\text{sinc}^2(\pi/N)$.

According to the above discussion, the design methodology is straightforward: 1) choose the desired G_m-C LPF[2] with half the bandwidth of the desired BPF; 2) substitute all the capacitors in the LPF by their N-phase switched-capacitor counterparts with baseband capacitance of $1/N^{\text{th}}$ of the ones used in the LPF counterpart. The design methodology is illustrated in Fig. 4.4(a). A few examples of this methodology are given in Fig. 4.4(b). One example where the methodology should be utilized indirectly is illustrated in Fig. 4.4(c) [112] due to the fact that its low-frequency counterpart is not band-limited. Of course in this case, if the voltage around the switched capacitor part is taken as output, the methodology can be exploited to find the transfer function there, T(s), and finally the actual output transfer function can be found by (1-T(s)). It should be noted that all the components inside the box in Fig. 4.4(a) should be memory-less. As it was discussed, all the baseband capacitors in the LPF counterpart should be converted to their switched-capacitor counterparts in the resultant N-path BPF. However, the parasitic capacitors introduced by active components to the internal nodes of the filter can not be converted to their switched-capacitor counterpart. This deviation in the synthesis can potentially distort the passband shape of the N-path BPF. The effect of parasitic capacitance on N-path filters is explored in subsection 4.2.4 and we will deal with this issue in section 4.4. Finally, in contrast to LTI circuits, cascading two N-path filter sections does not necessarily result in the product of their individual gains, as shown in Appendix 4.A.

4.2.3 The Effect of Switch Resistance on N-path Filters

In reality, the switches have a non-zero switch resistance and this potentially can modify the transfer function of the resultant filter (Fig. 4.5(a)). To find the effect of switch resistance on the frequency response of the filter, the LPF counterpart of the filter is illustrated in Fig. 4.5(b) (substitution of all the switched-capacitor sections by a capacitor of N times their baseband capacitance). Here, the transfer function of the filter from its input voltage source, $V_{\text{in}}(\Delta\omega)$ to every baseband voltage, $V_{\text{BB}i}(\Delta\omega)$,

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[2]Any types of LPF such as op-amp RC can be used, however because the active devices should operate at high frequencies, G_m-C is preferred over the other types of LPF.
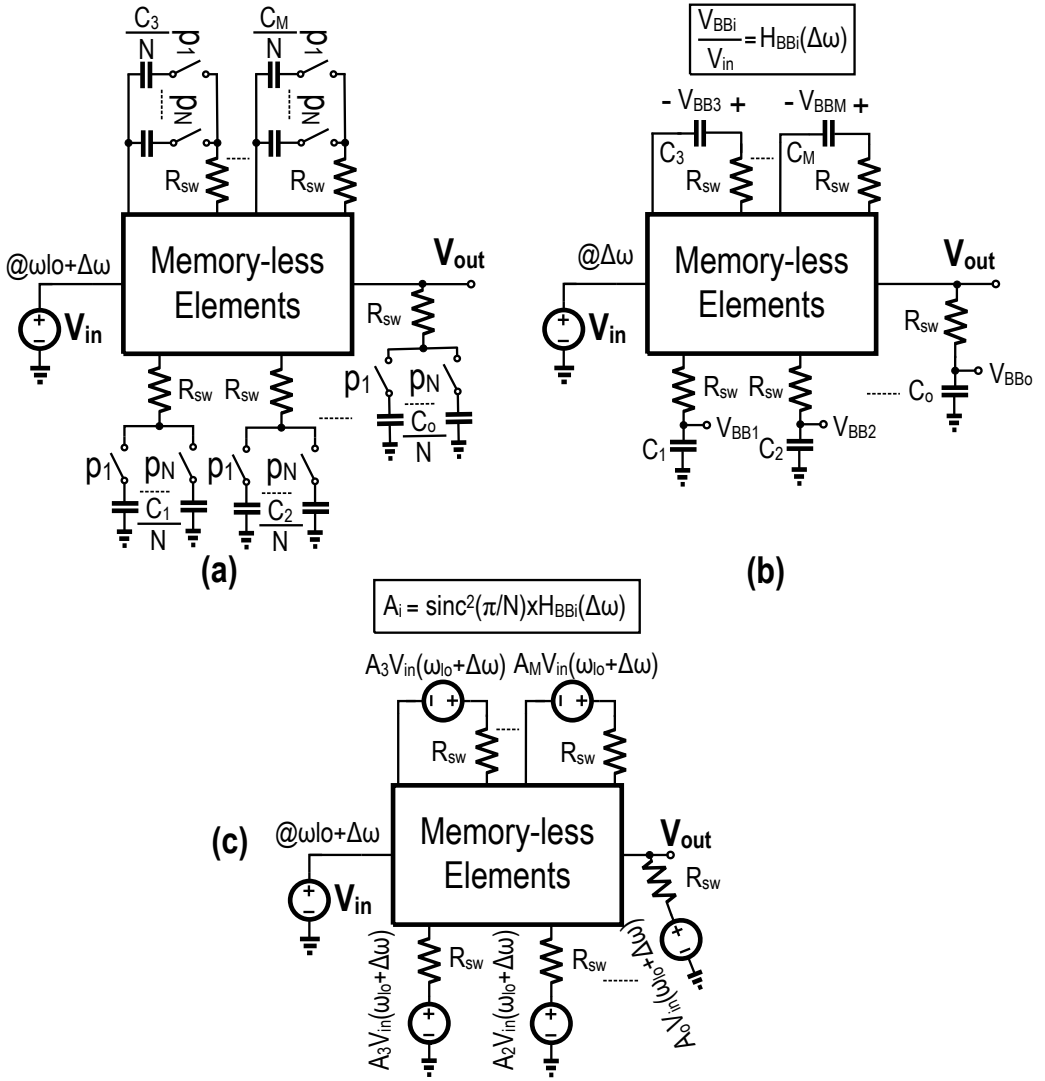
Figure 4.5: (a) The effect of switch resistance, R_{sw}, on the transfer function of the filter (b) The LPF version of the N-path filter (c) The transfer function of the filter can be found as a superposition of the different voltage sources.

$i = [1, \text{M}]$ is calculated, $\text{H}_{\text{BB}i}(\Delta\omega)$, where M is the number of switched-capacitor sections of the BPF. Afterwards, each of these transfer functions will be transformed to around the clock frequency by a scaling factor, $\text{A}_i(\omega_{lo} + \Delta\omega) = \text{sinc}^2(\pi/\text{N}) \times \text{H}_{\text{BB}i}(\Delta\omega)$. Now, the total transfer function of the filter can be found by superposition as illustrated in Fig. 4.5(c). Therefore in general, a non-zero switch resistance: 1) modifies the poles of the filter; and 2) introduces some unwanted zeros into the transfer function of the filter (due to the superposition). For typical values of switch resistance, these unwanted zeros are far outside the passband of the filter. These zeros are responsible for the limited stop-band rejection of the filter. In general, because the non-zero switch resistance reduces the bandwidth of baseband capacitors, it reduces the Q-factor of the resultant filter.

4.2.4 The Effect of Parasitic Capacitance on N-path Filters

Because an N-path filter emulates an RLC tank, it is intuitively expected that the addition of parasitic capacitance at the input node of the filter only lowers the center frequency of the filter and does not introduce loss. However as will be shown here, it does introduce voltage loss. As we will see, if the input impedance of the filter is modeled by an RLC tank, the values of L and C are independent from the value of the parasitic capacitance. However, the resistive part of the RLC tank decreases as C_p increases. The transfer function of the filter shown in Fig. 4.6(a) around f_{lo} is [98, 101]:

$$\text{T}(\omega_{lo} + \Delta\omega) = \frac{\text{Y}_s(j(\omega_{lo} + \Delta\omega))}{\frac{\text{NC}_{BB}j\Delta\omega}{\text{sinc}^2(\pi/\text{N})} + \sum_{m=-\infty}^{+\infty} \frac{\text{Y}_s(j(\text{N}m+1)\omega_{lo})}{(1+m\text{N})^2}}. \tag{4.4}$$

If the series in the denominator of (4.4) is called Y_{eff} [98], then Y_{in} in Fig. 4.6(a) will be:

$$\text{Y}_{\text{in}} = \text{Re}(\text{Y}_{\text{eff}}) - \text{Re}(\text{Y}_s) + j \times \left(\frac{\text{NC}_{BB}\Delta\omega}{\text{sinc}^2(\pi/\text{N})} + \text{Im}(\text{Y}_{\text{eff}}) - \text{Im}(\text{Y}_s)\right). \tag{4.5}$$

Now by exploiting (4.4-4.5), the effect of parasitic capacitance on the performance of the N-path filter is investigated (Fig. 4.6(b)). The N-path filter illustrated in Fig. 4.6(b) is converted to the circuit shown in Fig. 4.6(c) to be compatible with Fig. 4.6(a). In this case, $\text{Y}_s(s)$ is $1/(\text{R}_s + \text{R}_{sw}) \times (\text{R}_s\text{C}_p s + 1)/(\text{R}_s||\text{R}_{sw}\text{C}_p s + 1)$. Consequently, the transfer function of the circuit in Fig. 4.6(c) from V_{in} to V_x can be found by:

$$\text{T}(\omega_{lo} + \Delta\omega) = \frac{1}{j\text{R}_s||\text{R}_{sw}\text{C}_p\omega_{lo} + 1} \times \frac{1}{\text{R}_s + \text{R}_{sw}} \times \frac{1}{j\left(\frac{\text{NC}_{BB}\Delta\omega}{\text{sinc}^2(\frac{\pi}{\text{N}})} + \text{Im}\right) + \text{Re}}, \tag{4.6}$$
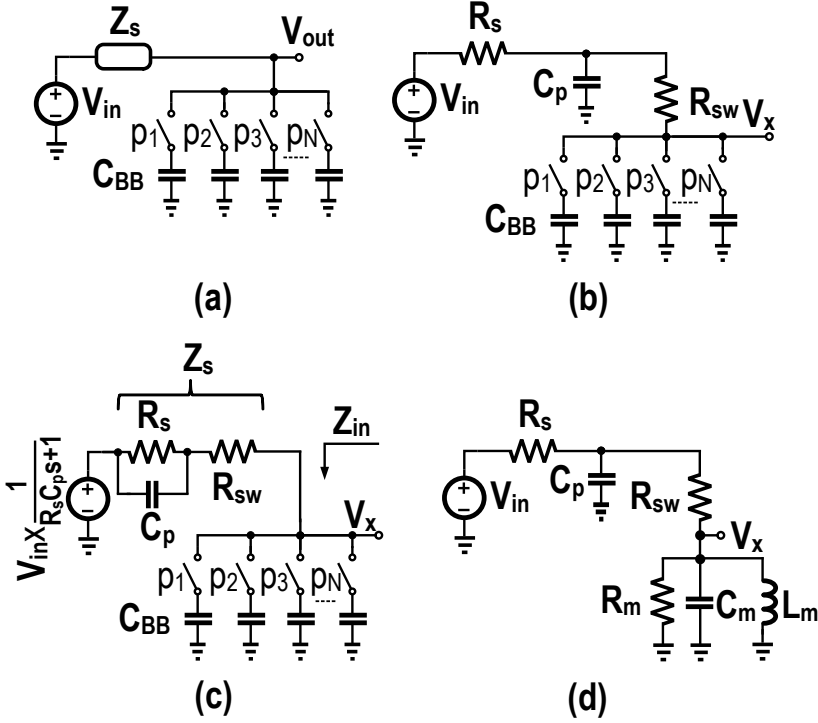
Figure 4.6: (a) An N-path filter with general source impedance (b) The effect of parasitic capacitance C_p on N-path filter (c) Making the model compatible with part (a) (d) The effect of parasitic capacitance on the input impedance of N-path filter.

where Re and Im are (4.7) and (4.8), respectively.

$$\text{Re} = \frac{1}{\text{R}_s + \text{R}_{sw}} \times \sum_{n=-\infty}^{+\infty} \frac{1 + (1+n\text{N})^2(\text{R}_s||\text{R}_{sw})\text{R}_s\text{C}_p^2\omega_{lo}^2}{(1+n\text{N})^2[1 + (1+n\text{N})^2(\text{R}_s||\text{R}_{sw})^2\text{C}_p^2\omega_{lo}^2]} \tag{4.7}$$

$$\text{Im} = \frac{1}{\text{R}_s + \text{R}_{sw}} \times \sum_{n=-\infty}^{+\infty} \frac{(\text{R}_s - \text{R}_{sw}||\text{R}_s)\text{C}_p\omega_{lo}}{(1+n\text{N})[1 + (1+n\text{N})^2(\text{R}_s||\text{R}_{sw})^2\text{C}_p^2\omega_{lo}^2]} \tag{4.8}$$

As can be deduced from (4.6), the center frequency of the filter (4.9) shifts to the lower frequency.

$$\omega_c = \omega_{lo} - \frac{\text{Im} \times \text{sinc}^2(\frac{\pi}{\text{N}})}{\text{NC}_{BB}} \tag{4.9}$$
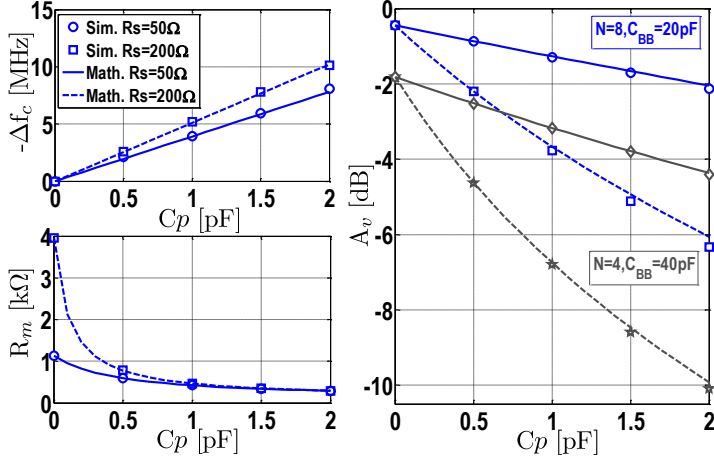
Figure 4.7: The effect of parasitic capacitance on N-path filters: change in the center frequency of the filter Δf_c, input impedance at center frequency of the filter R_m, and voltage gain A_v for two different values of source resistance, $R_s = 50 \ \Omega$ and $200 \ \Omega$ as a function of parasitic capacitance C_p; $f_{lo} = 1$ GHz, $R_{sw} = 10 \ \Omega$, $C_{BB} = 20$ pF and N = 8; Also, the effect of parasitic capacitance on voltage gain of filter is shown for N = 4 and 8.

$$|T(\omega_c)| = \frac{1}{(R_s + R_{sw}) \times Re \times \sqrt{(R_s||R_{sw})^2 C_p^2 \omega_{lo}^2 + 1}} \tag{4.10}$$

The input impedance of the filter can be modeled by an RLC tank (Fig. 4.6(d)) where:

$$\frac{1}{R_m} = Re - \frac{1}{R_s + R_{sw}} \frac{1 + (R_s||R_{sw})R_s C_p^2 \omega_{lo}^2}{1 + (R_s||R_{sw})^2 C_p^2 \omega_{lo}^2}, \tag{4.11}$$

$$C_m = \frac{NC_{BB}}{2\text{sinc}^2(\pi/N)}, \ L_m = \frac{1}{C_m \times \omega_{lo}^2}. \tag{4.12}$$

Therefore the only thing that is modified by parasitic capacitance is the tank's resistance R_m which reduces as C_p increases and this stands for the raise in the loss of the filter. The effect of parasitic capacitance on change of the center frequency (4.9), and the impedance of the filter at its center frequency (4.11) for two different values of source resistance, $R_s = 50 \ \Omega$ and $200 \ \Omega$, $f_{lo} = 1$ GHz, $R_{sw} = 10 \ \Omega$, $C_{BB} = 20$ pF and N = 8 is shown in Fig. 4.7. Moreover, the effect of input parasitic capacitance on the voltage gain of the N-path filter for two different number of phases, N = 4 and 8, is illustrated in Fig. 4.7. As can be seen, the effect of parasitic capacitance is much

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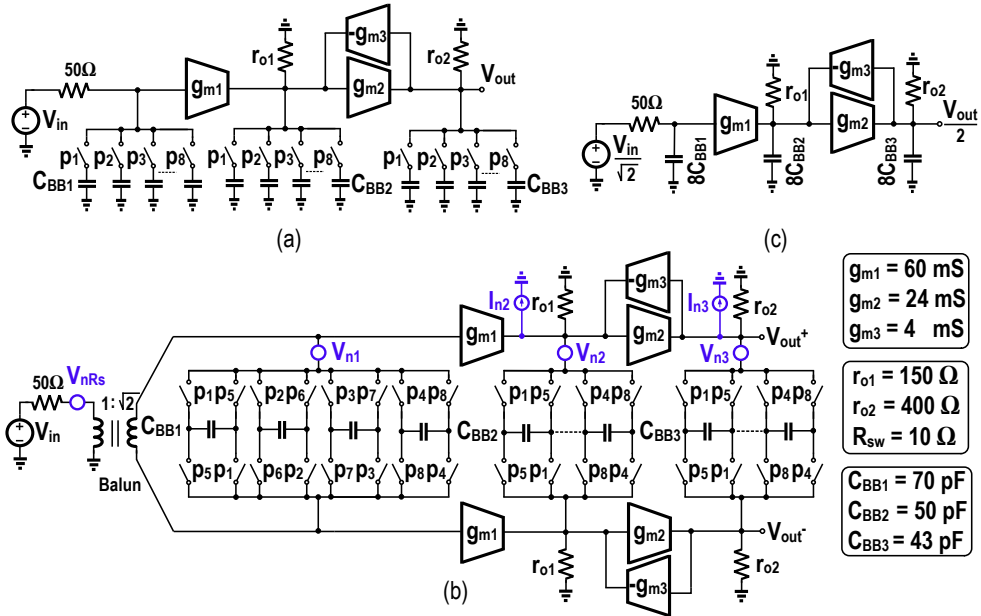
Figure 4.8: (a) Proposed 6th order N-path BPF (b) Using differential circuit to be resilient to common mode noise and utilization of differential clocking scheme to eliminate the gain of the filter at DC and even harmonics of the clock frequency (c) The LPF counterpart of the filter to be used in the design process.

more pronounced in the case of lower number of phases and higher values of source resistance. This effect can be explained intuitively. Every time a switch is on, there is a charge sharing between the baseband capacitor and the parasitic capacitor, leading to energy loss and hence lowering the gain of filter. This effect can be mitigated by lowering the harmonic content of the filter by increasing the number of phases.[3] The effect of parasitic capacitance on an active N-path filter can be deduced from the above discussion: 1) it lowers the effective impedance of the internal nodes of the filter and consequently de-Qs the filter shape; 2) due to the reduction of the center frequency of switched-capacitor sections, it introduces an extra phase shift to each node of the filter which potentially can lead to an unwanted peaking in the passband shape of the filter. These effects are exacerbated as the switching frequency increases.

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[3]Please note that increasing the number of phases also increases the parasitic capacitance of the switches. Therefore, in a case where the parasitic capacitance of the switches is the main contributor, increasing the number of phases is not beneficial.

4.3 Design of the Proposed Filter

To reduce the number of active components and hence lowering the power consumption and increase the dynamic range of the filter, the first gyrator in the proposed filter (Fig. 4.2(d)) is substituted by a single G_m cell. In this way, the filter can be seen as stagger tuning a 2nd and a 4th order BPF (Fig. 4.8(a)). The gyrator is realized using two G_m cells. In contrast to conventional gyrator design, two different values have been assigned to the feedforward and return G_ms of the gyrator. As we will see later, the noise contribution of the gyrator will be lowered and at the same time a decent amount of gain can be achieved. We chose 8 phases in our design. As discussed previously, increasing the number of phases is beneficial in reducing the folding-back issues and hence decreasing the NF of the filter (less noise-folding from higher harmonics of f_{lo}) and lowering the spurs. However, there are tradeoffs among folding-back, maximum achievable frequency and dynamic power consumption. A differential structure is exploited to combat common-mode disturbance. To eliminate bandpass filtering at even harmonics of the clock frequency, a differential clocking scheme is utilized (Fig. 4.8(b)). In this way, the even Fourier coefficients of the effective clock signals are zero and hence there is no gain at DC and other even harmonics of the filter. To save area, capacitors are made differential.

4.3.1 Transfer Function of the Filter

As discussed in the design methodology, by substituting each switched-capacitor section with an equivalent baseband capacitance of NC_{BBi}, the single-ended LPF counterpart of the filter is shown in Fig. 4.8(c) will result. Transfer function of this filter by ignoring the effect of the switch resistance is described by:

$$T_{\mathrm{LPF}}(s) = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{T_0}{(1 + s/p_1)(as^2 + bs + 1)} \tag{4.13}$$

where

$$T_0 = \frac{\sqrt{2}g_{m1}g_{m2}}{g_{m2}g_{m3} + g_{o1}g_{o2}} \tag{4.14}$$

$$\begin{aligned}
p_1 &= \frac{1}{8C_{BB1}R_s} \\
a &= \frac{8^2 C_{BB2}C_{BB3}}{g_{o1}g_{o2} + g_{m2}g_{m3}} \\
b &= \frac{8C_{BB3}}{g_{o2} + g_{m2}g_{m3}/g_{o1}} + \frac{8C_{BB2}}{g_{o1} + g_{m2}g_{m3}/g_{o2}}.
\end{aligned} \tag{4.15}$$

Because $g_{m2}g_{m3} \gg g_{o1}g_{o2}$, (4.14) can be simplified to $T_0 = \sqrt{2}g_{m1}/g_{m3}$. The g_{m1} is chosen to be 60 mS, for noise requirement. The g_{m3} is 4 mS which leads to a

voltage gain of 25.5 dB. Now we will find the transfer function of the filter including the effect of switch resistance using the proposed methodology.

$$T(\omega_{lo} + \Delta\omega) = \frac{\sqrt{2}\text{sinc}^2(\frac{\pi}{8})}{1 + D \times R_{sw}^2 + (g_{o1} + g_{o2})R_{sw}} \times$$

$$\Big[g_{m1}g_{m2}R_{sw}^2 H_{1bb}(\Delta\omega) - g_{m2}R_{sw}^2 H_{2bb}(\Delta\omega) + \tag{4.16}$$

$$(1 + R_{sw}g_{o1})H_{outbb}(\Delta\omega) + \frac{R_{sw}^3 g_{m1}g_{m2}}{\text{sinc}^2(\frac{\pi}{8})(R_{sw} + R_s)}\Big]$$

where

$$H_{1bb}(s) = \frac{1}{1 + 8C_{BB1}(R_{sw} + R_s)s}$$

$$H_{2bb}(s) = \frac{-g_{m1}(1 + 8C_{BB1}R_{sw}s)[g_{o2} + 8C_{BB3}s(1 + g_{o2}R_{sw})]}{[1 + 8C_{BB1}(R_{sw} + R_s)s](As^2 + Bs + D)} \tag{4.17}$$

$$H_{outbb}(s) = \frac{g_{m1}g_{m2}(1 + 8C_{BB1}R_{sw}s)(1 + 8C_{BB2}R_{sw}s)}{[1 + 8C_{BB1}(R_{sw} + R_s)s](As^2 + Bs + D)}$$

$$\frac{A}{g_{o1}g_{o2} + g_{m2}g_{m3}} = a \times [1 + (g_{o1} + g_{o2})R_{sw} + (g_{o1}g_{o2} + g_{m2}g_{m3})R_{sw}^2], \tag{4.18}$$

$$\frac{B}{g_{o1}g_{o2} + g_{m2}g_{m3}} = b + 8(C_{BB2} + C_{BB3})R_{sw}, \tag{4.19}$$

and D is $g_{o1}g_{o2} + g_{m2}g_{m3}$. For typical values of switch resistance, the zeros of the transfer function are far outside the passband of the filter and they can be ignored in the design procedure. Now based on the equations described above, we design a center frequency tunable BPF with bandwidth of 9 MHz. The values of capacitors and G_m cells are shown in Fig. 4.8. In transistor-level implementation, relatively high value of g_{m1} leads to low r_{o1}. In the actual realization, two negative resistors have been added to the internal nodes of the filter (see section 4.4) to increase and control r_{o1} and r_{o2}. Because it is not desirable to use large amount of negative admittance (reduction in DR and increase in P_{DC}), a value of 150 Ω and 400 Ω are chosen for r_{o1} and r_{o2}, respectively. Although exploiting higher values of $r_{o1,2}$ reduces the required value of baseband capacitance for a certain bandwidth, it amplifies the effect of parasitic capacitances because the associated decrease in R_m (see Fig. 4.7) is relatively stronger. In general, the non-zero switch resistance lowers the Q-factor of the filter. The simulated transfer function of the filter with component values shown in Fig. 4.8 is illustrated in Fig. 4.9(a). Moreover, the effect of 2.5% reduction in the duty-cycle of the clocks is shown in Fig. 4.9(a) which is a reduction in the stopband
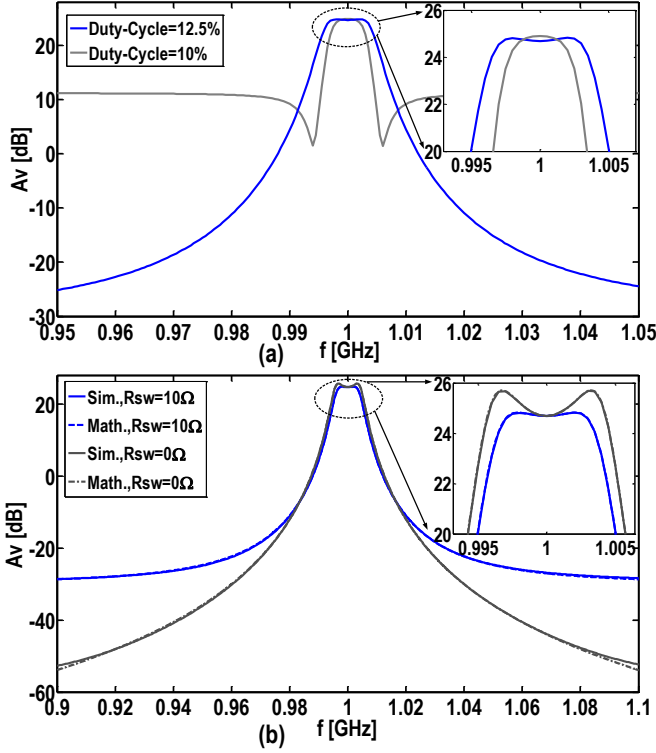
Figure 4.9: (a) The simulated transfer function of the filter for $R_{sw} = 10 \; \Omega$ and Duty-cycle of 10% and 12.5% b) A comparison between simulation and mathematical derivation (4.16) for R_{sw} of 0 Ω and 10 Ω.

rejection of the filter and reduction in the bandwidth of the filter. (The baseband capacitors see their equivalent resistance for a smaller amount of time.) In fact, because there are N time-slots with width of $T_{lo} (D_{ideal} - D_{real})$, the gain difference between passband and stopband will be $\text{sinc}^2(\frac{\pi}{N})/[N (D_{ideal} - D_{real})]$ for $D_{ideal} > D_{real}$ which in our case is 14 dB (Fig. 4.9(a)).[4]

For perfect duty cycles, the stop-band rejection, A_{sb}, (the difference between the pass-band and stop-band voltage gain) of the filter can be found using the simplified circuit shown in Fig. 4.10 and it is described in (4.20). For the values used in our design, the stop-band rejection is 56 dB. A technique to eliminate the effect of switch-resistance on the ultimate rejection of the filter is discussed in Appendix 4.B.

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[4]In reality, by correct choice of the DC bias voltage of the gate of switches and the rise and fall time of the clock signals (typically in the range of 10-20 ps), we can be sure that always one of the switches is on.
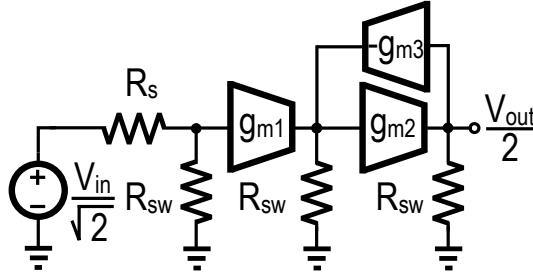
Figure 4.10: A simplified schematic of the filter to calculate the stop-band gain of the filter; the baseband capacitors are shorted to ground for frequencies far from the pass-band of the filter and $\sqrt{2}$ is the voltage gain of the BALUN.

$$\frac{1}{A_{sb}} = \text{sinc}^2\left(\frac{\pi}{8}\right) \times \left(1 + \frac{1}{R_{sw}^2 g_{m2} g_{m3}}\right) \times \left(1 + \frac{R_s}{R_{sw}}\right) \qquad (4.20)$$

The simulated transfer function of the filter is compared with its mathematical derivation (4.16) in Fig. 4.9(b) for two different values of switch resistance (0 Ω and 10 Ω) and as can be seen they match very well. As can be seen, non-zero switch resistance reduces the Q-factor of the filter.

4.3.2   NF of the Filter

Here, the noise behavior of the filter is analyzed. At first, it is required to find the transfer function of different noise sources to the output node of the filter (Fig. 4.8(b)). $V_{n1,2,3}$ represent the switch resistance noise of different sections and $I_{n2,3}$ represent the noise contribution of the G_m cells and the r_{o1} and r_{o2} on each node. The same technique that is illustrated in Fig. 4.5 can be exploited here. The only difference here is that for the input signals (e.g., noise sources) located at $(1+kN)f_{lo}$, the baseband signals are scaled by $N^2|a_1 a_{(-1-kN)}| = \text{sinc}^2\left(\pi/N\right)/(1+kN)$. The input signals located at $(1+kN)f_{lo}$ are downconverted to the baseband signals by the mixing operation of the switches with gain of $N|a_{(-1-kN)}|$ and then these downconverted signals are upconverted to f_{lo} by the mixing operation of the switches with gain of $N|a_1|$. The transfer functions of different noise sources $\omega_{\text{noise}} = (1 + kN)\omega_{lo} + \Delta\omega$, $k \in \mathbb{Z}$ to the output node ($\omega_{\text{out}} = \omega_{lo} + \Delta\omega$) are described in (4.21).

$$\frac{\mathrm{V_{out}}|_{\omega_{lo}+\Delta\omega}}{\mathrm{I}_{n2}|_{(1+8k)\omega_{lo}+\Delta\omega}} = \begin{cases} \mathrm{sinc}^2(\frac{\pi}{8})\mathrm{Z}_{2x} + \gamma & k = 0 \\ \frac{\mathrm{sinc}^2(\frac{\pi}{8})}{1+8k}\mathrm{Z}_{2x} & k \neq 0 \end{cases}$$

$$\frac{\mathrm{V_{out}}|_{\omega_{lo}+\Delta\omega}}{\mathrm{I}_{n3}|_{(1+8k)\omega_{lo}+\Delta\omega}} = \begin{cases} \mathrm{sinc}^2(\frac{\pi}{8})\mathrm{Z}_{3x} - \mathrm{R}_{sw}\beta & k = 0 \\ \frac{\mathrm{sinc}^2(\frac{\pi}{8})}{1+8k}\mathrm{Z}_{3x} & k \neq 0 \end{cases}$$

$$\frac{V_{out}|_{\omega_{lo}+\Delta\omega}}{\mathrm{V}_{n1}|_{(1+8k)\omega_{lo}+\Delta\omega}} = \begin{cases} \mathrm{sinc}^2(\frac{\pi}{8})\mathrm{H}_{1x} - \frac{\gamma g_{m1}\mathrm{R}_s}{\mathrm{R}_s+\mathrm{R}_{sw}} & k = 0 \\ \frac{\mathrm{sinc}^2(\frac{\pi}{8})}{1+8k}\mathrm{H}_{1x} & k \neq 0 \end{cases} \tag{4.21}$$

$$\frac{V_{out}|_{\omega_{lo}+\Delta\omega}}{\mathrm{V}_{n2}|_{(1+8k)\omega_{lo}+\Delta\omega}} = \begin{cases} \mathrm{sinc}^2(\frac{\pi}{8})\mathrm{H}_{2x} - \alpha & k = 0 \\ \frac{\mathrm{sinc}^2(\frac{\pi}{8})}{1+8k}\mathrm{H}_{2x} & k \neq 0 \end{cases}$$

$$\frac{V_{out}|_{\omega_{lo}+\Delta\omega}}{\mathrm{V}_{n3}|_{(1+8k)\omega_{lo}+\Delta\omega}} = \begin{cases} \mathrm{sinc}^2(\frac{\pi}{8})\mathrm{H}_{3x} + \eta & k = 0 \\ \frac{\mathrm{sinc}^2(\frac{\pi}{8})}{1+8k}\mathrm{H}_{3x} & k \neq 0 \end{cases}$$

where α is $\mathrm{R}_{sw}g_{m2}/(1+\mathrm{DR}_{sw}^2+(g_{o1}+g_{o2})\mathrm{R}_{sw})$, γ is $g_{m2}\alpha$, η is $1-g_{m3}\gamma-\mathrm{R}_{sw}g_{o2}\beta$, and β is $(1+g_{o1}\mathrm{R}_{sw})/(1+\mathrm{DR}_{sw}^2+(g_{o1}+g_{o2})\mathrm{R}_{sw})$. Moreover, H_{1x} is $\alpha(\mathrm{H}_{2bb}-g_{m1}\mathrm{Z}_{22})+\beta(g_{m1}\mathrm{Z}_{out2}-\mathrm{H}_{outbb})-\mathrm{R}_sg_{m1}\gamma\mathrm{H}_{1bb}/(\mathrm{R}_{sw}+\mathrm{R}_s)$, H_{2x} is $-\alpha\mathrm{H}_{22}+\beta\mathrm{H}_{out2}$, H_{3x} is $\alpha(g_{m3}\mathrm{Z}_{22}-g_{o2}\mathrm{Z}_{23})-\beta(g_{m3}\mathrm{Z}_{out2}-g_{o2}\mathrm{Z}_{out3})$, Z_{2x} is $-\alpha\mathrm{Z}_{22}+\beta\mathrm{Z}_{out2}$ and Z_{3x} is $-\alpha\mathrm{Z}_{23}+\beta\mathrm{Z}_{out3}$. Also,

$$\mathrm{Z}_{22}(\Delta\omega) = \frac{g_{o2} + 8j\mathrm{C}_{\mathrm{BB3}}(1 + g_{o2}\mathrm{R}_{sw})\Delta\omega}{\mathrm{den}(\Delta\omega)}$$

$$\mathrm{Z}_{out2}(\Delta\omega) = \frac{g_{m2}(1 + 8\mathrm{C}_{\mathrm{BB2}}s\mathrm{R}_{sw})}{\mathrm{den}(\Delta\omega)}$$

$$\mathrm{Z}_{23}(\Delta\omega) = \frac{-g_{m3}(1 + 8\mathrm{C}_{\mathrm{BB3}}s\mathrm{R}_{sw})}{\mathrm{den}(\Delta\omega)}$$

$$\mathrm{Z}_{out3}(\Delta\omega) = \frac{g_{o1} + 8j\mathrm{C}_{\mathrm{BB2}}(1 + g_{o1}\mathrm{R}_{sw})\Delta\omega}{\mathrm{den}(\Delta\omega)} \tag{4.22}$$

$$\mathrm{H}_{22}(\Delta\omega) = \frac{-\mathrm{D}(1 + 8j\mathrm{C}_{\mathrm{BB3}}\mathrm{R}_{sw}\Delta\omega)}{\mathrm{den}(\Delta\omega)}$$

$$\mathrm{H}_{out2}(\Delta\omega) = \frac{-8jg_{m2}\mathrm{C}_{\mathrm{BB2}}\Delta\omega}{\mathrm{den}(\Delta\omega)}.$$

$$\mathrm{den}(\Delta\omega) = -\mathrm{A}(\Delta\omega)^2 + j\mathrm{B}\Delta\omega + \mathrm{D}.$$

Now, by knowing the transfer function of all the noise sources to the output voltage from $f_{\mathrm{in}} = |1 + 8k|f_{lo}$ to $f_{\mathrm{out}} = f_{lo}$ (4.21), the total output voltage noise of the filter, including all the folding-back components, can be found as shown in Fig. 4.11. (4.23) is used in subsection 4.4.1 to calculate the noise figure of the filter.
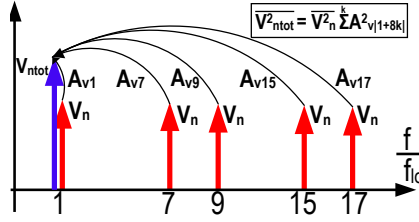
Figure 4.11: Folding-back of noises located at $|1 + 8k|f_{lo}$ to f_{lo}.

$$0.5\overline{V_{\text{out,n}}^2}|_{\omega_{lo}+\Delta\omega} = \left(\sum_{i=2}^{3} \overline{I_{ni}^2}|Z_{ix}|^2 + \sum_{i=1}^{3} \overline{V_{ni}^2}|H_{ix}|^2 \right) \times$$

$$\left(\text{sinc}^2(\frac{\pi}{8}) - \text{sinc}^4(\frac{\pi}{8}) \right) + \overline{V_{n1}^2} \left| \text{sinc}^2(\frac{\pi}{8})H_{1x} - \frac{\gamma g_{m1}R_s}{R_s + R_{sw}} \right|^2$$

$$+ \overline{V_{n2}^2} \left| \text{sinc}^2(\frac{\pi}{8})H_{2x} - \alpha \right|^2 + \overline{V_{n3}^2} \left| \text{sinc}^2(\frac{\pi}{8})H_{3x} + \eta \right|^2 + \tag{4.23}$$

$$\overline{I_{n2}^2} \left| \text{sinc}^2(\frac{\pi}{8})Z_{2x} + \gamma \right|^2 + \overline{I_{n3}^2} \left| \text{sinc}^2(\frac{\pi}{8})Z_{3x} - \beta R_{sw} \right|^2 +$$

$$2kTR_s \left(|T|^2 + \left(\text{sinc}^{-2}(\frac{\pi}{8}) - 1 \right) \left| T - \frac{\sqrt{2}\gamma R_{sw}g_{m1}}{R_{sw} + R_s} \right|^2 \right)$$

4.4 Realization

The filter was realized in CMOS LP 65 nm technology. The schematic of the proposed filter is illustrated in Fig. 4.12(a). As discussed in section 4.2, in the methodology, it is assumed that all the components except the baseband capacitors are memory-less elements. However, in reality this is not the case and G_m cells and switches contribute a large amount of parasitic capacitance to the internal nodes of the filter. These parasitic capacitances and their associated extra phase shifts (In section 4.2, it was shown that besides introducing loss, the parasitic capacitance lowers the effective center frequency of the filter which is equivalent to extra phase shift) can potentially distort the passband shape of the filter. This is the same phenomenon that also occurs in bandpass G_m-C filters [42]. In this work, our aim was to alleviate this issue with minimum additional components. A simple yet effective way to attain this purpose is to use a Miller compensation method, C_F, as shown in Fig. 4.12. It is possible here due to the uni-lateralization made by G_{m1} and having a decent amount of gain in the filter. The intuitive explanation is given in Fig 4.12(d). Two effects are involved in the operation of the Miller compensation: 1) it reduces the effect of parasitic
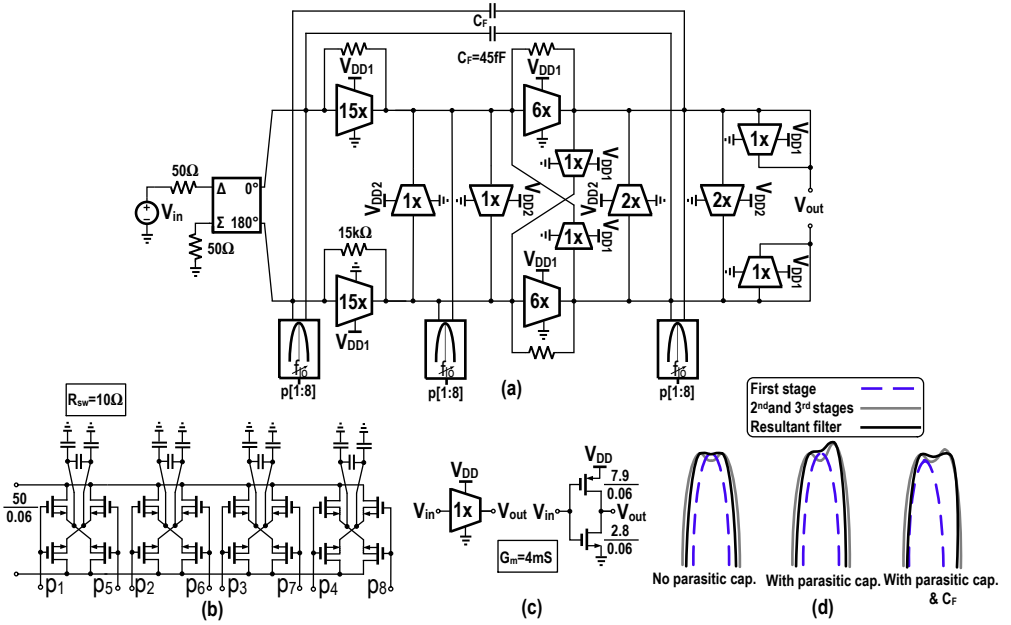
Figure 4.12: (a) The transistor level schematic of the filter (b) Implementation of the switches and baseband capacitors (c) The unit G_m cell that is used in the filter with different scaling factors (d) An intuitive explanation of the operation of the proposed Miller-compensation method.

capacitors on the output node of the filter due to its bandwidth enhancement effect at output node of the filter and hence leads to reduction of the passband ripple of the 4th order section; 2) it reduces the center frequency of the 2nd order section and hence the peaking part will see less gain and eventually this leads to the elimination of the peaking in the passband shape of the resultant filter (see subsection 4.4.1). Each switch in the filter (Fig. 4.12(b)) is sized (W/L = 50μm/60nm) to obtain an on resistance of around 10 Ω. Each NMOS switch is in a separate p-well with its bulk and source tied together, avoiding an increase in the threshold voltage of the transistor.[5] Large switches are used to reduce their noise, nonlinearity, mismatch between them and to increase the stopband rejection of the filter. Nevertheless, increasing the size of the switches will introduce more parasitic capacitance to the filter nodes which can lead to distortion of the passband shape of the filter. Moreover, large switch transistors increase the dynamic power consumption and the LO leakage to the input port of the filter. Because the drain and source of each switch have a DC bias of

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[5]The parasitic capacitance of the well is in parallel with the baseband capacitors and therefore it is not important.

Figure 4.13: Obtaining 8 non-overlapping clocks by utilization of a modulo-8 counter; D flip-flops are implemented using transmission gates.

0.6 V ($V_{DD}/2$), for proper operation (high linearity and low on resistance) of the switches, the low and high levels of the clock signals should be raised by 0.6 V. The clock signals are ac-coupled to the gate of each switch which has a high ohmic resistor to a bias voltage of 0.75 V ($5V_{DD}/8$). The ac-coupling capacitors are sized large enough to minimize the voltage loss due to the capacitive voltage division between the ac-coupling capacitor and the gate capacitance of the switches.[6] The baseband capacitors are realized by a combination of accumulation-mode NMOS and MOM capacitors.

All the G_m cells are based on a self-biased inverter [39] unit-cell (Fig. 4.12(c)) using minimum channel-length transistors with different scaling factors. To reduce the parasitic capacitance of the G_ms, LVT (low V_{th}) transistors are used in the design which leads to 30% reduction in parasitic capacitance compared to the SVT (standard V_{th}) case.[7] However, using LVT transistors leads to more power consumption. Because $g_m = I_{DC}/(V_{DD}/2 - V_{th})$, therefore as V_{th} decreases, the required DC current for the same g_m increases accordingly. Two negative resistors made of inverters are added to the circuit to control the impedance level of the internal nodes of the filter namely r_{o1} and r_{o2} in the design (see Fig. 4.8(c)). These negative resistors have a separate supply voltage (AV_{DD2}) with nominal value of 1.2 V. To make the

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[6]The voltage loss can be compensated by an slight increase of the DC bias voltage of the clock signals.

[7]The difference between the threshold voltage of the two cases is 0.1 V.

Figure 4.14: On-chip measurement interface of the proposed filter.

common-mode positive feedback which exists in the gyrator stable, two diode connected inverters are added to the output nodes of the filter. All the G_ms together draw about 11.7 mA from the 1.2 V. A modulo-8 ring counter is used to obtain 8 non-overlapping clock signals with 12.5 % duty cycle. The simplified block diagram of the clock generator [108] is shown in Fig. 4.13 where a master clock at 8 times the switching frequency is applied externally. Due to its lower power consumption and higher speed, D flip-flops based on transmission gates have been exploited [108]. Fig. 4.14 illustrates the on-chip measurement interface of the proposed filter which is also used in the simulations.

Fig. 4.15(a) illustrates the effect of Miller compensation method on the passband shape of the filter. Without Miller compensation, there is a 1.5 dB peaking in the passband of the filter. The optimum value of the Miller capacitor (45 fF) is found using simulations. The simulated transfer function of the proposed filter in the whole tuning range is illustrated in Fig. 4.15(b). The utilized value of AV_{DD2} (a separate voltage source for negative resistors) is shown for each clock frequency. As discussed before, the parasitic capacitance at each node of the filter modifies the equivalent resistance of that node. This effect is frequency dependent which means that as clock frequency reduces, the Q-factor of the filter increases. This leads to higher ripples in
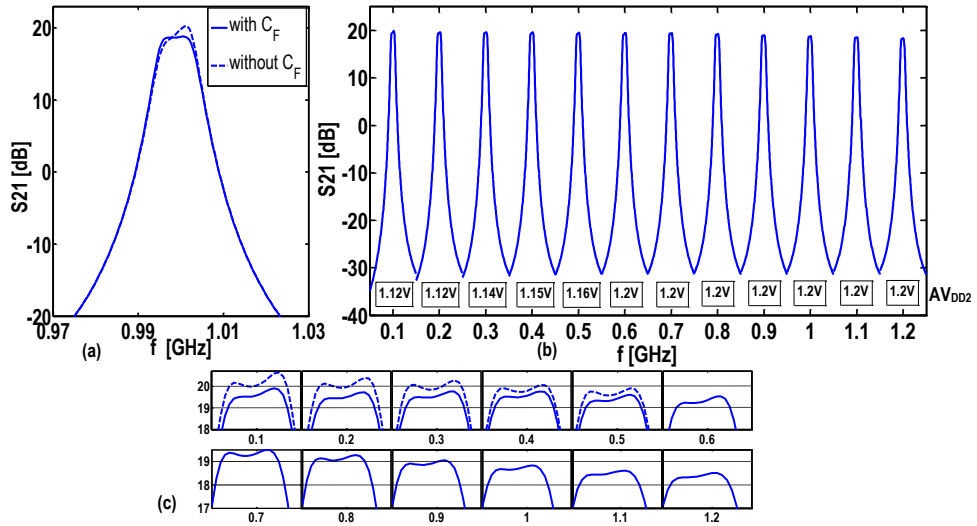
Figure 4.15: (a) The simulated transfer function of the filter with and without additional feedback capacitors C_F (b) The simulated transfer function of the filter in the whole tuning range; the utilized value of the separate supply voltage AV_{DD2} is also depicted for each clock frequency. Nominal AV_{DD2} is 1.2 V. (c) The passband details of the filter in the whole tuning range; also the passband shape of the filter in the case of fixed AV_{DD2} is shown for comparison (the dashed ones).

the passband of the filter for low clock frequencies. As a remedy, the supply voltage of the negative resistors is reduced for low clock frequencies. Albeit the amount of modification in AV_{DD2} is less than $\leq 7\%$. The simulated passband details of the filter shape in the whole tuning range is depicted in Fig. 4.15(c) which includes the case where the AV_{DD2} is fixed (1.2 V). The passband gain of the filter varies by 1 dB in the tuning range and the maximum passband ripple is 0.3 dB. As can be seen in Fig. 4.15(c), the passband ripple of the filter without any modification ($AV_{DD2} = 1.2$ V) is ≤ 0.6 dB. In reality, due to PVT variations, the value of the G_m cells changes, leading to a modifcation in the bandwidth of the filter. However, by tuning the supply voltage of the G_m cells, this can be corrected.

4.4.1 Simulation Results

The simulated NF of the filter is shown in Fig. 4.16 for two cases: 1) there is no parasitic capacitance in the circuit and 2) there are parasitic capacitance and Miller compensation. Moreover, the mathematical derivation of the noise figure in the case of no parasitic capacitance (4.23) is illustrated for comparison which is in close agreement
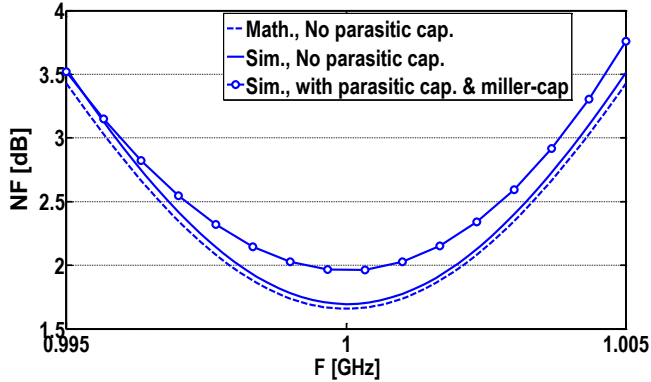
Figure 4.16: A comparison between the simulated and calculated NF in the case of no parasitic capacitance and simulate NF in the case of parasitic capacitance and Miller compensation.

with simulation. The increased capacitance at input port of the filter due to the Miller capacitance and its associated loss (see section 4.2) is the cause of 0.3 dB degradation in the NF of the filter compared to the case of no parasitics. The simulated NF of the filter in the whole tuning range is around 2 dB.

4.5   Measurements

The chip micrograph of the proposed filter is illustrated in Fig. 4.17. The chip has been fabricated in CMOS LP 65 nm technology and the active area of the filter is about 0.27 mm^2. The chip is mounted in a QFN32 package and tested on a printed circuit board. The measured transfer function of the filter in the whole tuning range (0.1 GHz to 1.2 GHz) and the passband shape of the filter are demonstrated in Fig. 4.18. The maximum passband ripple of the filter in the whole tuning range is less than 0.6 dB. The negative resistances of the filter are slightly changed by tuning their supply voltages (AV$_{DD2}$) ($\leq 8\%$) over the whole tuning range. However, without any modifications, the pass-band ripple is still less than 1 dB (≤ 0.6 dB in the simulation) over the whole tuning range. The measured stop-band rejection of the filter is 59 dB. The bandwidth of the filter is about 8 MHz which is equivalent to a Q-factor of 125 at center frequency of 1 GHz. Because the bandwidth of N-path filters is constant, as the center frequency of the filter reduces, the Q-factor of the filter will decrease. In this case, the Q-factor of the filter varies from 12.5 at $f_{lo} = 0.1$ GHz to 150 at $f_{lo} = 1.2$ GHz. The passband gain of the filter is about +25 dB after de-embedding the loss of the common-drain buffers calculated from simulation. The measured S$_{11}$
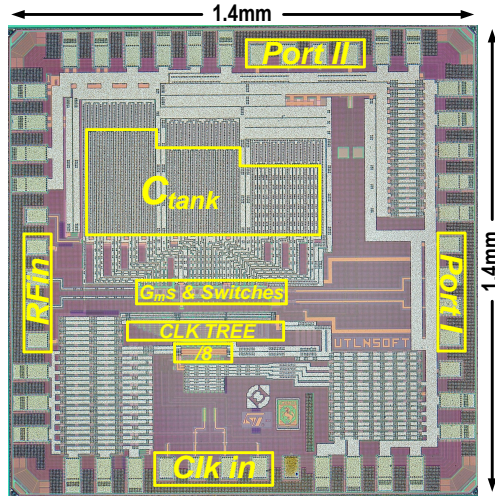
Figure 4.17: CMOS LP 65 nm chip micrograph indicating functional blocks

varies between -5 dB and -8 dB, in the passband of the filter over the clock frequency range.

The measured NF of the filter is shown in Fig. 4.19(a). It varies from 2.6 dB to 3.1 dB in the tuning range. The filter can attain a low NF because of: 1) the exploitation of asymmetric gyrators; 2) a relatively high value of g_{m1}; 3) the utilization of a very small amount of negative admittance; 4) a low switch resistance; and 5) the utilization of 8 phases which leads to less harmonic-folding of the noise at higher harmonics of the clock frequency. The measured out-of-band $\text{IIP}_3(\text{OOB})$ and 1dB blocker compression point $B_{-1\text{dB,CP}}$ for different offset frequencies from $f_{\text{lo}} = 1$ GHz are illustrated in Fig. 4.19(b). For IIP_3 measurements, two tones which are located at frequency of $f_{\text{lo}} + \Delta f$ and $f_{\text{lo}} + 2\Delta f$ have been used. For $B_{-1\text{dB,CP}}$ measurements, the input power of the blocker located at $f_{\text{lo}} + \Delta f$ that leads to a 1 dB reduction in the passband gain of the filter is reported. The measured $\text{IIP}_3(\text{OOB})$ of $+26$ dBm and 1dB blocker compression point $B_{-1\text{dB,CP}}$ of $+7$ dBm are achieved at Δf of only 50 MHz and f_{lo} of 1 GHz. To demonstrate the resilience of the filter to large out-of-band blockers, the transfer function of the filter at $f_{\text{lo}} = 1$ GHz is measured with and without a continuous-wave blocker with an input power of $+2.3$ dBm located only $+20$ MHz far from the center frequency of the filter and it is shown in Fig. 4.19(c). The filter can achieve excellent out-of-band linearity because of: 1) the first section being "passive" and hence the first G_m already receives a 2nd-order filtered signal and the further filtering in the subsequent stages; 2) the very linear differential I/V characteristic of an inverter when loaded with low impedance [39, 113]. The
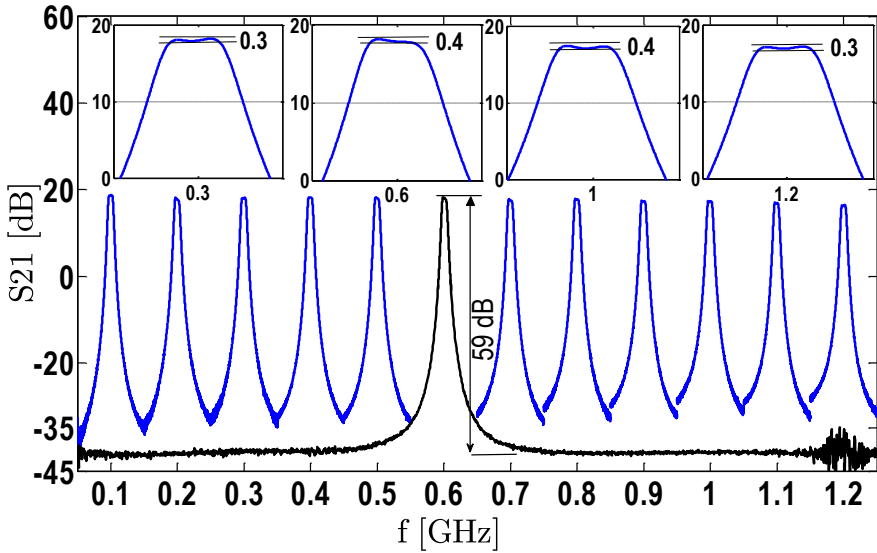
Figure 4.18: Measured transfer function of the filter in whole tuning range for the variable AV_{DD2} (the same as the values used in the simulations) (0.1 GHz to 1.2 GHz); in addition, the pass-band shape of the filter at some center frequencies are shown.
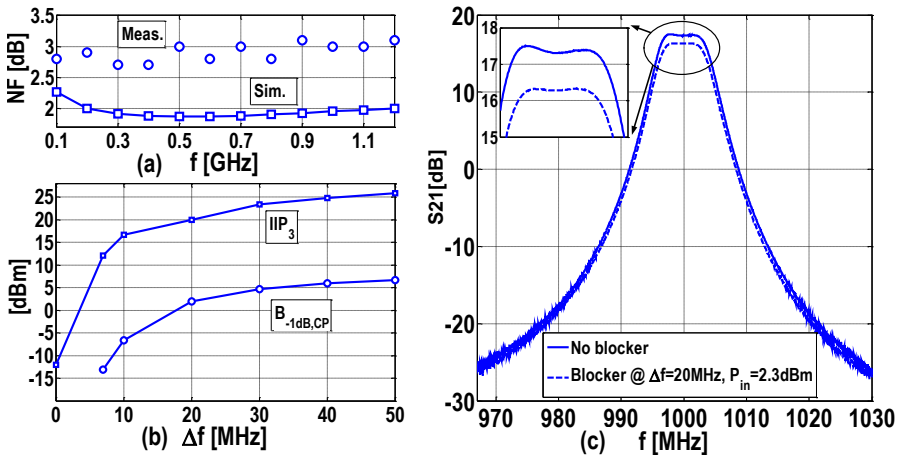
Figure 4.19: (a) Measured NF of the filter over the whole tuning range (b) Measured out-of-band IIP_3 and 1dB blocker compression point $B_{-1dB,CP}$ of the filter for different values of offset frequency from center frequency of the filter ($f_{lo} = 1$ GHz) (c) Measuring the transfer function of the filter at f_{lo} of 1 GHz with and without a large out-of-band blocker with input power of +2.3 dBm at offset frequency of 20 MHz.

Table 4.1: A comparison Between Simulation and Measurement Results

	Measurement	Simulation
Gain [dB]	+25	+26
NF [dB]	$2.6 - 3.1$	$1.9 - 2.3$
IIP3$_{\text{IB}}$ [dBm]	-12	-14
IIP3$_{\text{OOB}}$ [dBm] (Δf= +50MHz)	+26	+30
P$_{-1\text{dB}}$ [dBm]	-23	-26
B$_{-1\text{dB,C}}$ [dBm] (Δf= +50MHz)	+7	+7.5
BW [MHz]	8	9
Ripple [dB]	≤ 0.6	≤ 0.3

measurement results are compared with simulation results in Table 4.1. The in-band linearity of the filter is limited by inverters. However for out-of-band signals, all nodes of the filter see a 10Ω resistance to the ground. Due to the large amount of attenuation provided by the switched-capacitor sections, the nonlinearity contribution of the inverters is reduced considerably. In this case, the linearity of the filter will be limited to both the linearity of the switches and inverters. The filter draws 11.7 mA and the LO chain draws 3 to 36 mA from 1.2 V in the whole tuning range. The LO feedtrough to the input port of the filter is less than -64 dBm at f_{lo} of 1 GHz. As discussed previously, folding-back starts from $7f_{lo}$. However, due to mismatches between switches and clock signals (the mismatch between the clock signals is the major contributor [98, 103, 106].), folding-back also occurs from $3f_{lo}$ and $5f_{\text{lo}}$ with measured normalized gain of -54 dB and -68 dB, respectively.

If the same filter were designed as a conventional G_m-C filter, to synthesize the three resonators, 12 additional inverters would be required. Moreover, the output impedance of these extra G_m cells would reduce the impedance level at internal nodes of the filter and hence more negative admittance would be necessary. This would lead to an increase in power consumption of the filter and reduction of the DR of the filter. Also, it would need an additional PLL to correct the center frequency of the filter over process corners [42] which is in contrast to N-path filters where the center frequency of the filter is determined by the switching frequency. In the case of Q-enhanced LC filters, due to the low Q-factor of the on-chip inductors, a large amount of negative resistance would be needed which would definitely reduce the DR of the filter and more importantly LC filters are not tunable and process scalable. Finally, it can be said the DR of the proposed BPF is the same as its LPF counterpart which contains a much lower number of active devices compared to BP G_m-C filters.

The filter is compared with state-of-the-art integrated filters [20, 98, 106] and complete receivers [103, 113, 114] in Table 4.2. Compared to [106], much better

Table 4.2: Comparison Table

	This work	[98]	[20]	[106]	[114]	[103]	[113]
Circuit Type	Filter				Receiver		
Tech.[c][nm]	65	65	250	65	40	65	40
$f_{cen.}$ [GHz]	$0.1 - 1.2$	$0.4 - 1.2$	2.14	$0.1 - 1$	$0.4 - 6$	2	$0.08 - 2.7$
$IIP3_{oob}$[dBm]	$+26$[a]	$+29$[a]	N.A.	$> +14$	$+10$	-6.3	$+13.5$
$B_{1dB,CP}$[dBm]	$+7$	N.A.	N.A.	$> +2$	-8	N.A.	< 0
NF[dB]	2.8	10	19	$3 - 5$	3	5.8	2
Gain[dB]	$+25$	$+3.5$	0	-2	$+70$	$+55.8$	$+70$
BW[MHz]	8	20	60	35	$0.4 - 30$	4	N.A.
Ripple[dB]	< 0.6	< 0.4	0.7	-	-	-	-
Order	6	4	6	2	2[b]	6	2[b]
Ult.-Rej.[dB]	59	> 55	> 30	15	< 15[b]	50	< 15[b]
V_{DD}[V]	1.2	1.2/2.5	2.5	1.2	2.5	1.2/2.5	1.3
P_{DC}[mW]	$P_{ana.} = 14.4$ $P_{dig.}=3.6\text{-}43$	$12.8 - 21.4$	17.5	$2 - 20$	$75 - 137.5$	21mA	$35 - 78$
Area[mm^2]	0.27	0.12	3.51	0.07	2	0.76	1.2

[a] $\Delta f = +50$ MHz.

[b] @ RF.

[c] CMOS.

pass-band shape, selectivity and stopband rejection are obtained. Compared to [103], better out-of-band linearity, filter shape and NF are accomplished. Compared to [98], the NF is improved by more than 7 dB. The proposed integrated tunable BPF can be used as a channel-select SAW-LNA hybrid which is tunable over a decade in frequency. Due to the isolation provided by G_{m1}, when a large out-of-band blocker is not present, it is possible to turn-off the first stage, lowering the dynamic power consumption and improving the NF of the filter.

4.6 Conclusion

A design methodology for synthesis of active N-path BPFs is introduced. Based on this methodology, a 0.1-to-1.2 GHz tunable 6th-order N-path channel-select filter in 65 nm LP CMOS is introduced. It is based on coupling N-path filters with gyrators, achieving a "flat" pass-band shape and high out-of-band linearity. A Miller compensation method is utilized to considerably improve the passband shape of the filter. The filter has 2.8 dB NF, $+25$ dB voltage gain, $+26$ dBm wideband IIP$_3$, $+7$ dBm $B_{1dB,CP}$ and 59 dB stop-band rejection. The analog and digital part of the filter draw 11.7 mA and $3 - 36$ mA from 1.2 V, respectively. The proposed filter only consists of inverters, switches and capacitors and therefore it is friendly with process scaling.
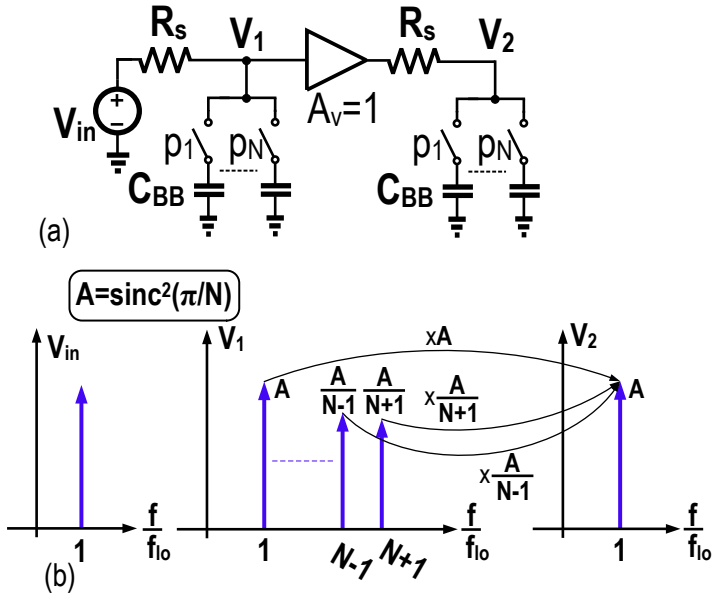
Figure 4.20: (a) A cascade of two identical N-path filters (b) A graphical representation of calculation of the total gain of the filter.

4.A Cascading Two N-path Filters

We already know that the gain of a simple N-path filter at its center frequency is $\text{sinc}^2(\pi/N)$. Accordingly, it may be thought that the gain of the cascade of two N-path filters shown in Fig. 4.20(a) should be $\text{sinc}^4(\pi/N)$. However based on the proposed methodology, also the gain of the cascaded one should be $\text{sinc}^2(\pi/N)$. What causes this discrepancy?

We should make two observations: 1) the first N-path filter other than making a signal at f_{lo} at node V_1, also produces signals at $(1+kN)f_{\text{lo}}$ with gain of $\text{sinc}^2(\pi/N)/(1+kN)$ [98]; 2) the second N-path filter other than passing the signal at f_{lo} without any frequency translation, also translates the produced harmonics of the first N-path filter at $(1+kN)f_{\text{lo}}$ to f_{lo} at node V_2 by gain of $\text{sinc}^2(\pi/N)/(1+kN)$ [98]. This process is illustrated graphically in Fig. 4.20(b). Therefore the gain of the filter is $\text{sinc}^4(\pi/N) \times \sum_{k=-\infty}^{\infty} 1/(1 + kN)^2$ which eventually can be simplified to $\text{sinc}^2(\pi/N)$. It is easy to show that the gain of an N-path notch filter [112] is $1-\text{sinc}^2(\pi/N)$ where as N decreases the depth of notch reduces. Now, consider the N-path filter illustrated in Fig. 4.21(a). Interestingly, it can be shown that the gain of the filter at f_{lo} at node V_2 is zero and does not depend on the number of phases. Based on the same observations we did above, the total gain of

Figure 4.21: (a) A cascade of a notch filter [112] and band-pass N-path filter (b) A graphical representation of calculation of the total gain of the filter at f_{lo}.

the filter can be found using Fig. 4.21(b). Consequently, the gain at f_{lo} will be $[1-\text{sinc}^2(\pi/N)]\times\text{sinc}^2(\pi/N)-\text{sinc}^4(\pi/N)\times\sum_{k\neq0}1/(1+kN)^2$ which finally can be simplified to 0.

4.B Elimination of the Effect of R_{sw} on Ultimate-Rejection of the Filter

It is possible to utilize the technique used in chapter 3 to suppress the effect of switch resistance on the stop-band rejection of the filter at the cost of doubling the dynamic power consumption. In this way, the out-of-band linearity of the filter improves. (For example, the first G_m cell would see higher stop-band rejection.) This is illustrated in Fig. 4.22(a). The LPF counterpart of the filter is shown in Fig. 4.22(b) which interestingly can be simplified to the circuit shown in Fig. 4.22(c). The values of the g_{m1n}, g_{m1n} and g_{m3n} are $g_{m1}\times r_{o1}/(r_{o1}+R_{sw})$, $g_{m2}\times r_{o2}/(r_{o2}+R_{sw})$ and $g_{m3}\times r_{o1}/(r_{o1}+R_{sw})$, respectively. The values of r_{o1n} and r_{o2n} are $r_{o1}+R_{sw}$ and $r_{o2}+R_{sw}$, respectively.
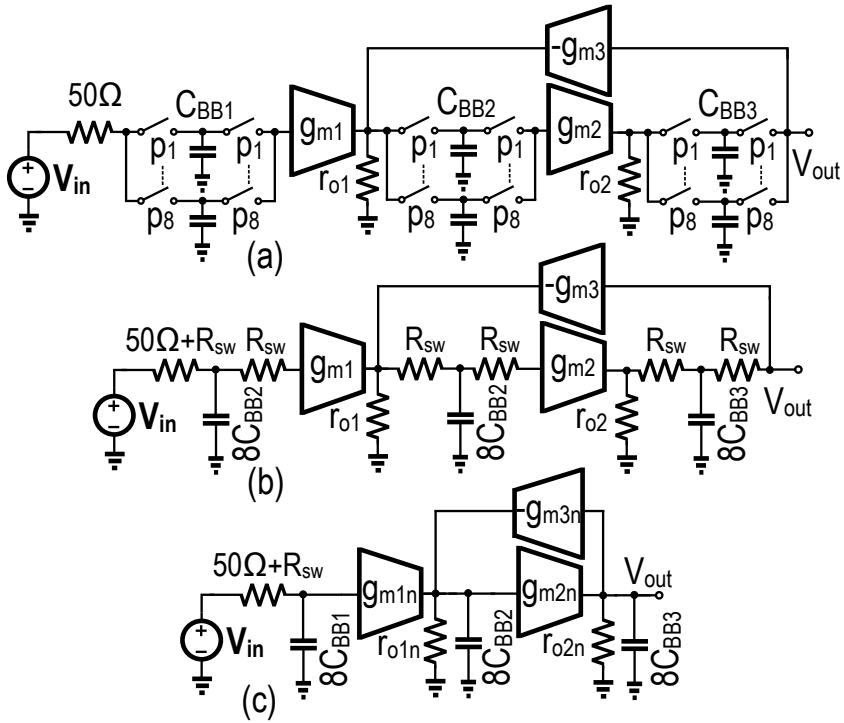
Figure 4.22: (a) Elimination of the effect of the switch resistance on the ultimate-rejection of the filter (b) Its LPF counterpart (c) A simplified version of the filter shown in part (b).

Chapter 5

Suppressing Harmonic Responses in N-path Filters

5.1 Introduction

A conventional N-path filter is illustrated in Fig. 5.1(a) where the on-resistance of the switches is modeled by a series resistance, R_{SW}. The clock signals, $p_i(t)$ $i = [1, N]$, are non-overlapping clocks with a duty cycle of 1/N. The input RF signals located around the clock frequency, f_{lo}, will be downconverted to baseband due to the switching operation of the switches. These baseband signals are then filtered due to the lowpass filtering of the combination of baseband capacitors, C_{BB}, and the source resistance, R_S. Due to the transparency of the switches, these lowpass filtered baseband signals are upconverted to around the switching frequency at node V_{out}. This procedure can be interpreted as a transformation of a LPF, which consists of C_{BB} and R_S, to a bandpass filter (BPF) with a center frequency equal to the switching frequency of the filter. In this way, N-path filters provide us with center-frequency tunable BPF where the bandwidth of the filter can be chosen independent of the center frequency by the value of C_{BB}.

Nonetheless, there are some issues associated with conventional N-path filters that need to be addressed, such as: 1) *limited stopband rejection* due to the non-zero switch resistance, R_{SW}; 2) *undesired folding-back* of the signals located at $|kN-1|f_{lo}$ to the center frequency of the filter, f_{lo}; and 3) *repetition of bandpass shapes* at higher harmonics of the clock frequency. For frequencies far from the passband of the filter, the impedance of the baseband capacitors, C_{BB}, is negligible and can be ignored. In this way, the filter can be simplified to a resistive divider shown in Fig. 5.1(b). As a consequence, the ultimate-rejection of the filter is limited to $R_{SW}/(R_{SW} + R_S)$ [98].
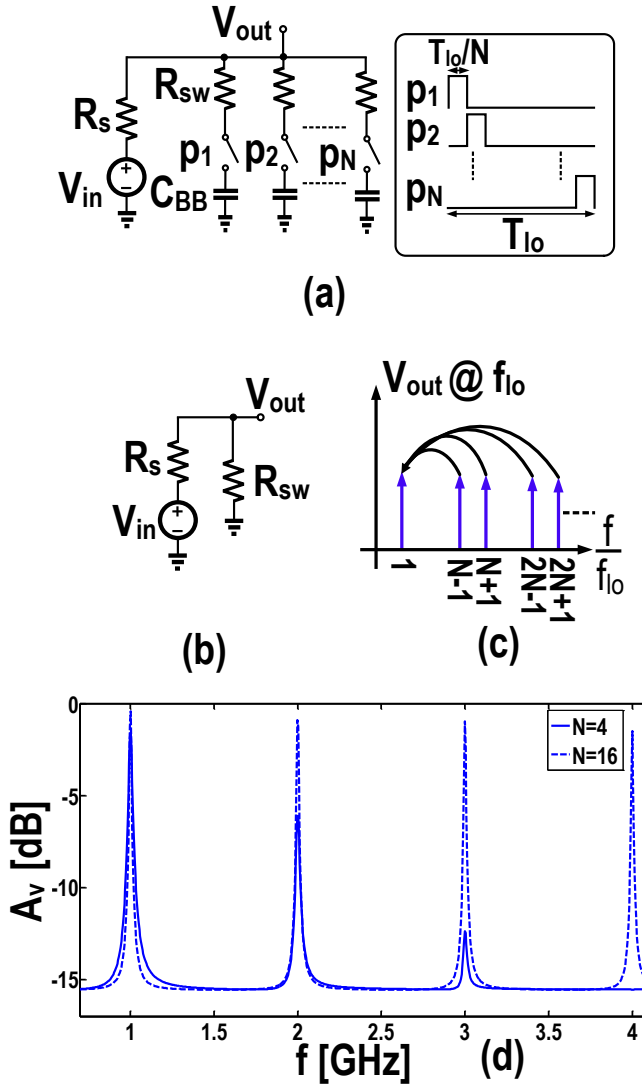
Figure 5.1: (a) A conventional N-path filter (b) A simplified schematic of the filter for out-of-band frequencies (c) Folding-back of signals located at $|kN-1|f_{lo}$ to f_{lo} (d) Comparing the transfer function of a conventional N-path filter for two different number of phases, N = 4 and 16.

Techniques to increase the stopband rejection of N-path filters have been presented in chapter 3 and 4 [98, 99, 100]. The problem of folding-back (Fig. 5.1(c)) can be alleviated by increasing the number of paths, N [98]. As mentioned before, in the ideal case where there is no mismatch between the different paths of the filter, folding-back starts from $(N-1)f_{lo}$. In the case of mismatch, which is mainly dominated by phase mismatch[1], folding-back is also present at lower harmonics of f_{lo} [102]. Practical realizations show that by a good layout, the mismatch induced folding-back gain can be made < -50 dB (chapter 3 and 4).

However, as the number of phases increases (to reduce the folding-back issues), the gain of the filter at higher harmonics of f_{lo} increases, which is undesirable. This is illustrated in Fig. 5.1(d). Blockers located at second and third harmonics of the clock frequency are passed with less attenuation when the number of phases is higher which can degrade the sensitivity of a receiver that is connected to the filter. To avoid this, a differential clocking scheme (chapter 4) and a subtraction method (chapter 3) have been exploited to eliminate the bandpass transfer functions of the filter at even harmonics of the clock frequency. However, signals located at third harmonic of f_{lo} are passed with little attenuation. It can be shown that the third harmonic rejection of an N-path filter is

$$\text{HR3} = 9 \times \frac{\sin^2\left(\dfrac{\pi}{N}\right)}{\sin^2\left(\dfrac{3\pi}{N}\right)} \tag{5.1}$$

which approaches 1 as N increases. As an example, according to (5.1), a conventional 8-path filter achieves 3.8 dB of 3rd harmonic rejection.

In this chapter, a technique to concurrently eliminate the bandpass filter shapes of a 6-path filter at $2kf_{lo}$ and $3kf_{lo}$, where $k \in \mathbb{Z}$, is proposed. A technique to provide input-matching for the proposed filter is introduced and a simple and intuitive method to find the transfer function of N-path filters over a large frequency range is presented which avoids the lengthy analysis described in literature so far. Using the proposed compact method, the transfer function and the input impedance of the filter are derived mathematically which are in close agreement with simulation results. Also, a simple and intuitive method to find the effect of parasitic capacitance on the transfer function of N-path filters is shown. Furthermore, to show the feasibility of the proposed technique, the simulation results of a possible implementation of the filter in CMOS 28 nm FDSOI are illustrated. The structure of this chapter is as follows: in section 5.2, a technique to concurrently cancel the bandpass filter shapes of a 6-path filter at $2kf_{lo}$ and $3kf_{lo}$ where $k \in \mathbb{Z}$ is proposed and a simple and intuitive method to find its transfer function over a large frequency range is presented. In section 5.3,

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[1]The mismatch between the baseband capacitors is quite low due to their large area.
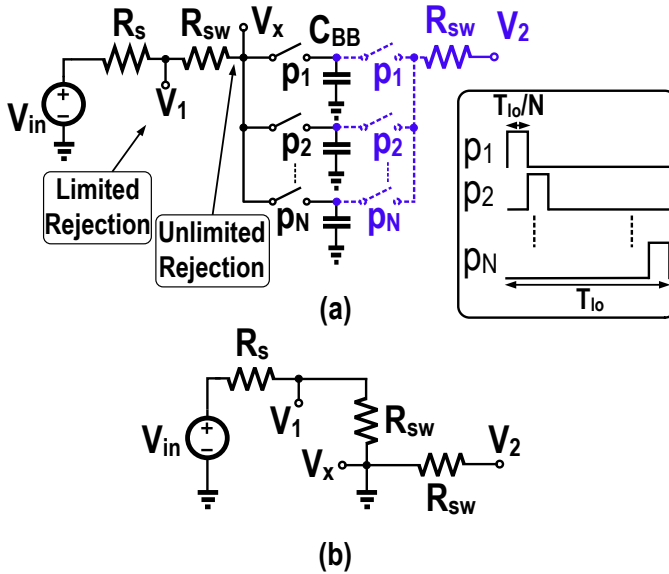
Figure 5.2: (a) Addition of a second set of switches to conventional N-path filters to eliminate the effect of the switch resistance R_{SW} on its stopband rejection (b) Simplified schematic of part (a) for input frequencies far from the passband of the filter.

a new technique to provide matching at input port of the filter will be discussed and its input impedance and transfer function will be derived mathematically. In the next section, an intuitive method to find the effect of parasitic capacitance on the transfer function of N-path filters is shown and the simulation results of the filter in CMOS 28 nm FDSOI are illustrated. Finally in section 5.5, we draw conclusions.

5.2 Elimination of Bandpass Shapes at Higher Harmonics of f_{lo}

5.2.1 An N-path Filter with Large Stopband Rejection

A conventional N-path filter is illustrated in Fig. 5.2(a) where the on-resistance of all the switches, which are the same, is lumped to one virtual resistance [101, 102, 19]. Although the stopband rejection is limited to $R_{SW}/(R_{SW} + R_S)$ at node V_1, it is not restricted at virtual node of V_x.[2] This filtering characteristic at node V_x can be

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[2]By virtual, we mean that it is not physically accessible.

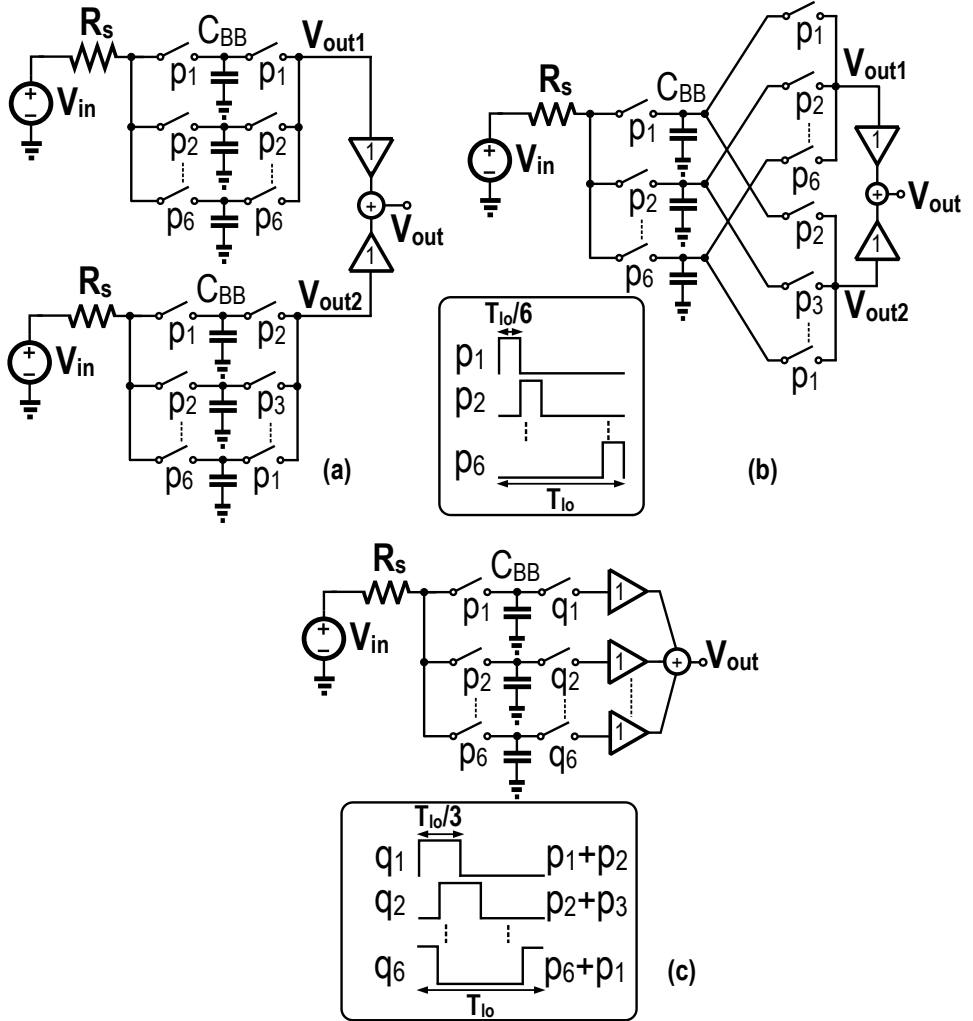Figure 5.3: (a) Addition of the output of two 6-path filters where the clock phases of the second set of switches of the lower path are shifted by $\pi/3$ compared to the upper one (b) Combining the first sections of the two filter (c) The filter can be seen as a 6-path filter where the clock signals of the second set of switches are $q_i(t)$, $i = [1, 6]$; these clock signals have a duty cycle of $1/3$.

exploited by using a second set of switches (chapter 3)[98, 99]. If the second set of switches does not conduct current, then V_2 is close to V_x.[3] For frequencies far from the passband of the filter, the impedance of the baseband capacitors is negligible and can be ignored. In this way, the filter can be simplified to a resistive divider shown in Fig. 5.2(b) which clearly shows that high-rejection at node V_x is inherited by node V_2. In this chapter, we utilize this technique to obtain a large stopband rejection, and we extend it to reduce the harmonic transfer of the filter.

5.2.2 Elimination of Bandpass Shapes at $3f_{\text{lo}}$

Interestingly, the introduced second set of switches can be further utilized to cancel some of the bandpass shapes of the filter at higher harmonics of the clock frequency. As an example, we demonstrate a method to eliminate the bandpass shapes of a 6-path filter around $3kf_{\text{lo}}$. In Fig. 5.3(a), two 6-path filters with a second set of switches where the clock phases of the second set of switches of the lower path are shifted by $\pi/3$ compared to the upper one, are shown. In contrast to the upper part where the clock signals of the first and second set of switches are identical, in the lower part, each clock signal of the second set of switches is modified to the next adjacent clock signal. (e.g., $p_1(t) \rightarrow p_2(t)$, $p_2(t) \rightarrow p_3(t)$ and etc.) The outputs of these two 6-path filters are added together. The idea is that the output signals of the two paths should be added constructively around $f_{\text{in}} = f_{\text{lo}}$ and destructively around $f_{\text{in}} = 3f_{\text{lo}}$. Now, It is assumed that the transfer function of the filter at V_{out1} at $M\omega_{\text{lo}} + \Delta\omega$ can be described by $H(M\omega_{\text{lo}} + \Delta\omega)$. Because of the introduced extra phase-shift ($2\pi/6 = \pi/3$) in the lower part, the transfer function of the filter at V_{out2} for $M\omega_{\text{lo}} + \Delta\omega$ is $e^{-j\frac{M\pi}{3}}H(M\omega_{\text{lo}} + \Delta\omega)$. Therefore, the total transfer function of the filter at V_{out} in Fig. 5.3(a) for $M\omega_{\text{lo}} + \Delta\omega$ is:

$$\text{T}(M\omega_{\text{lo}} + \Delta\omega) = \left(e^{-j\frac{M\pi}{3}} + 1\right)\text{H}(M\omega_{\text{lo}} + \Delta\omega). \tag{5.2}$$

(5.2) tells us that the voltage gain of the filter is zero when the frequency of the input signal is $3kf_{\text{lo}}$ where $k \in \mathbb{N}$. Please note that the phase difference between the input and output signal V_{out} is $-\pi/6$. Because the baseband voltages of the upper and the lower part are exactly the same, it is possible to merge the two filters, together. In this way, the filter illustrated in Fig. 5.3(b) will result. For better insight into the operation of the filter, it can be simplified to the circuit shown in Fig. 5.3(c) where the clock signals of the second set of switches are $q_i(t)$, $i = [1, 6]$. As can be seen, these clock signals have a duty cycle of $1/3$ and therefore their Fourier coefficients b_i

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[3]In the case of a load resistance, R_L, V_2 will only be an attenuated version of V_x by $R_L/(R_L + R_{SW})$ and it does not lead to a reduction in the stopband rejection of the filter. (see subsection 5.2.3)
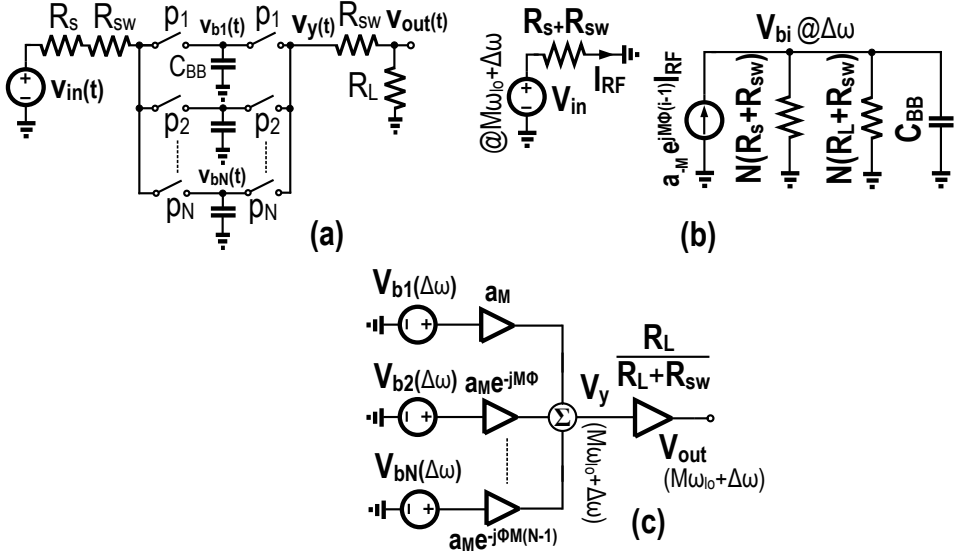
Figure 5.4: (a) An N-path filter with a second set of switches (b) A simple method to find the transfer function of the input voltage source to the baseband nodes (c) Calculation of the output voltage by a simple addition.

are zero for $i = 3k$. Now, we will introduce a compact method to calculate the exact transfer function of this filter in a large frequency range in an easy way.

5.2.3 Compact Analysis of an N-path Filter with Second Set of Switches

Here, we demonstrate a simple method to calculate the transfer function of conventional N-path filters as shown in Fig. 5.2 intuitively and simpler than the exhaustive and lengthy methods utilized in [101, 106]. A general N-path filter with a second set of switches is illustrated in Fig. 5.4(a). It is assumed that the baseband voltages in Fig. 5.4(a), $V_{\mathrm{b}i}$ $i = [1, N]$, only contain low-frequency (baseband) signals [83]. For the time that $p_i(t)$ is high, the current that goes to the baseband capacitor, C_{BB}, is $v_{\mathrm{in}}(t)/(R_{\mathrm{S}} + R_{\mathrm{SW}}) - v_{\mathrm{b}i}(t)\left[1/(R_{\mathrm{S}} + R_{\mathrm{SW}}) + 1/(R_{\mathrm{L}} + R_{\mathrm{SW}})\right]$. This can be regarded as the superposition of two currents: an RF current that is caused by $v_{\mathrm{in}}(t)$, and a baseband current caused by $v_{\mathrm{b}i}(t)$. This allows us to find the baseband voltage of one path, V_{bi}, with the help of the equivalent circuit in Fig. 5.4(b) where the left part works at RF and the right part works at baseband. Firstly, the RF current, $v_{\mathrm{in}}(t)/(R_{\mathrm{S}} + R_{\mathrm{SW}})$, will be converted to a baseband current due to the mixing operation with $p_i(t)$. Let us assume that the input signal is located at $M\omega_{\mathrm{lo}} + \Delta\omega$, $v_{\mathrm{in}}(t) = V_{\mathrm{in}}e^{j(M\omega_{\mathrm{lo}} + \Delta\omega)t}$. In this

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way, the magnitude of the effective baseband current that goes to the baseband capacitor due to the input voltage is $a_{(-M)}e^{jM\phi(i-1)}V_{in}/(R_S + R_{SW})$ where $a_{(-M)}e^{jM\phi(i-1)}$ is the Mth Fourier coefficient of $p_i(t)$ and ϕ is the phase difference between $p_1(t)$ and $p_2(t)$. Secondly, the baseband current, $-V_{bi}[1/(R_S + R_{SW}) + 1/(R_L + R_{SW})]$, is only present for $1/N^{th}$ of the time, so its effect on the baseband voltage V_{bi} can be modeled by two shunt resistors of $N(R_S + R_{SW})$ and $N(R_L + R_{SW})$. Therefore, $V_{bi}(\Delta\omega)$ as a function of input voltage, $V_{in}(M\omega_{lo} + \Delta\omega)$, will be:

$$V_{bi}(\Delta\omega) = \frac{a_{(-M)}e^{jM\phi(i-1)}I_{RF}N[(R_S + R_{SW})||(R_L + R_{SW})]}{jN[(R_S + R_{SW})||(R_L + R_{SW})]C_{BB}\Delta\omega + 1}$$
$$= Na_{(-M)}e^{jM\phi(i-1)}G(\Delta\omega)V_{in}(M\omega_{lo} + \Delta\omega), \tag{5.3}$$

where $G(\Delta\omega)$ is

$$G(\Delta\omega) = \frac{R_L + R_{SW}}{R_L + R_S + 2R_{SW}} \times \frac{1}{jN[(R_S + R_{SW})||(R_L + R_{SW})]C_{BB}\Delta\omega + 1}. \tag{5.4}$$

Afterwards, the voltage of all the baseband nodes, V_{bi}, are upconverted from $\Delta\omega$ to around $M\omega_{lo} + \Delta\omega$ at node V_{out} by the mixing operation with clock signals. As shown in Fig. 5.4(c), the contribution of each path to the node V_y is $V_{bi}a_M e^{-jM\phi(i-1)}$ which can be simplified to $N|a_M|^2 G(\Delta\omega)V_{in}(\omega_{lo} + \Delta\omega)$ using (5.3). Interestingly, the contribution of all the paths are identical and therefore the output voltage $V_{out}(\omega_{lo} + \Delta\omega)$ will be N times the contribution of one path as described in (5.5).

$$\frac{V_y(M\omega_{lo} + \Delta\omega)}{V_{in}(M\omega_{lo} + \Delta\omega)} = N^2|a_M|^2 G(\Delta\omega) = \text{sinc}^2\left(\frac{M\pi}{N}\right)G(\Delta\omega) \tag{5.5}$$

Because V_{out} is $R_L/(R_L + R_{SW})V_y$, the total transfer function of the filter will be:

$$H(M\omega_{lo} + \Delta\omega) = \text{sinc}^2\left(\frac{M\pi}{N}\right)G(\Delta\omega) \times \frac{R_L}{R_L + R_{SW}} \tag{5.6}$$

(5.6) is the transfer function of the N-path filter in Fig. 5.4(a) where the switched-capacitor section is substituted by an equivalent baseband capacitance of NC_{BB} as shown in Fig. 5.5, scaled by a scaling factor, $\text{sinc}^2\left(\frac{M\pi}{N}\right)$ and transformed to around Mf_{lo}. Therefore, to find the transfer function of an N-path filter at $M\omega_{lo} + \Delta\omega$: 1) substitute all the switched-capacitor sections with a capacitor with N times the baseband capacitance of that section; 2) calculate the transfer function of the resultant circuit; and 3) scale this transfer function by $\text{sinc}^2\left(\frac{M\pi}{N}\right)$ and then transform it to around $M\omega_{lo}$. In the case of no load impedance, the transfer function of the filter for
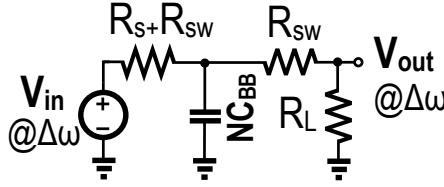
Figure 5.5: The LPF counterpart of the N-path filter shown in Fig. 5.4(a).
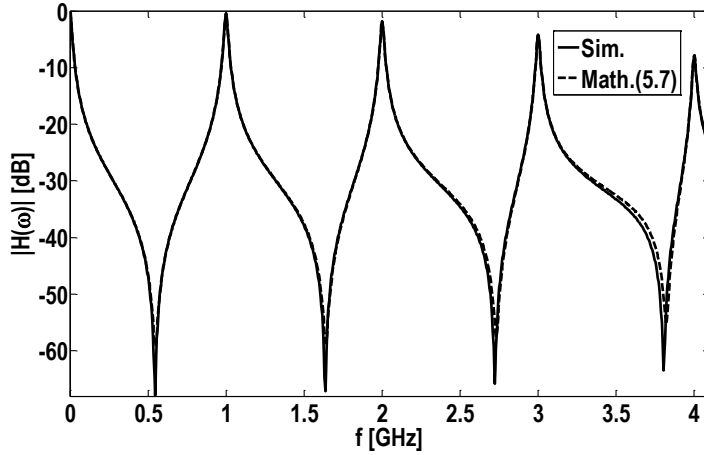
Figure 5.6: Comparing the simulated and calculated transfer function of an N-path filter with second set of switches; $f_{\text{lo}} = 1$ GHz, $R_S = 50 \, \Omega$, $R_{SW} = 10 \, \Omega$, $C_{BB} = 30$ pF and N = 8.

$0 \leq \omega \leq K\omega_{\text{lo}}$ can be found by the addition of the transfer function of the filter (5.6) for $-K \leq M \leq K$ as described by:

$$H(\omega) = \sum_{m=-K}^{K} \text{sinc}^2\left(\frac{m\pi}{N}\right) G(\omega - m\omega_{\text{lo}}) \tag{5.7}$$

where $G(\omega)$ is $1/[jN\,(R_S + R_{SW})\,C_{BB}\omega + 1]$. As an example, the transfer function of the filter with a second set of switches is shown in Fig. 5.6 for $f_{\text{lo}} = 1$ GHz, $R_S = 50 \, \Omega$, $R_{SW} = 10 \, \Omega$, C_{BB} of 30 pF and N = 8. It clearly shows that using a second set switches improves the stopband rejection of the filter compared to the conventional N-path filters where the stopband rejection is limited to 16 dB [106]. As can be seen, mathematical derivation (5.7) agrees well with simulation results. Interestingly, there are some transmission zeros in the total transfer function of the
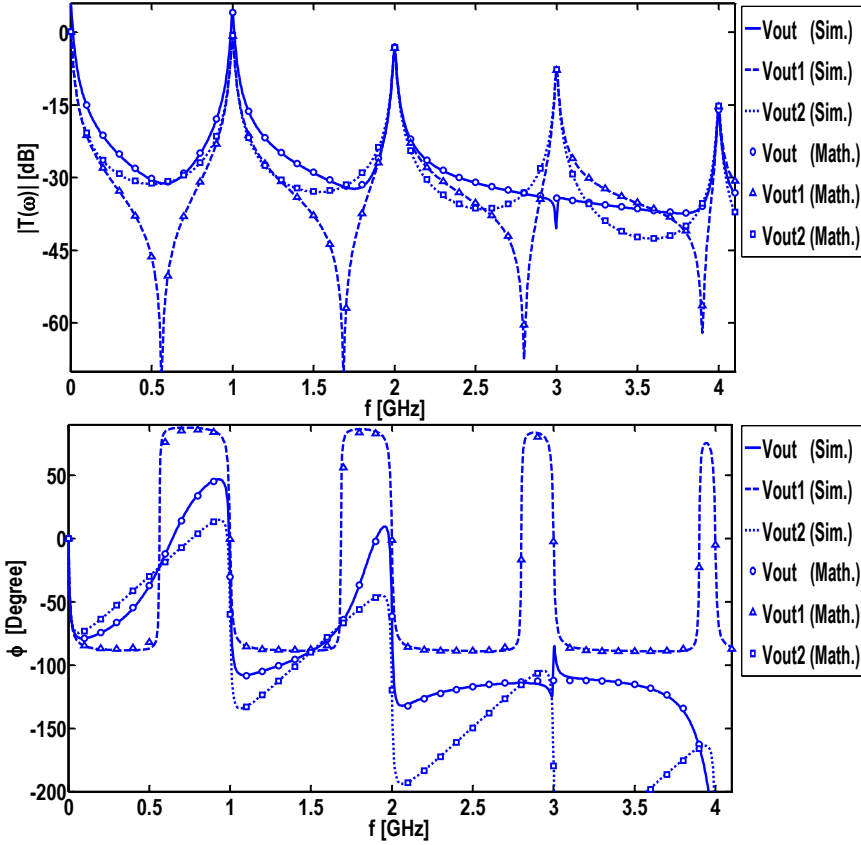
Figure 5.7: The simulated and calculated transfer function and phase of the filter at node V_{out1} (5.10), V_{out2} (5.11) and V_{out} (5.9) in Fig. 5.3(b) for $f_{lo} = 1$ GHz, $R_S = 50\ \Omega$, $R_{SW} = 10\ \Omega$ and $C_{BB} = 50$ pF.

filter. They can be explained intuitively: for $Kf_{lo} < f_{in} < (K+1)f_{lo}$, the phase of individual components of (5.7) for m $\leq$ K would be $-\pi/2$ and for m $\geq$ K + 1 would be $+\pi/2$ and hence anti-phase. Therefore, there exists a point in this frequency range where the transfer function of the filter drops to zero.

5.2.4 Concurrent Suppression of Bandpass Shapes at $2f_{lo}$ and $3f_{lo}$

Based on the compact analysis presented in the previous subsection, the transfer function of the filter shown in Fig. 5.3(b) at V_{out} for $M\omega_{lo} + \Delta\omega$ can be found by substituting (5.6) into (5.2) where N = 6 and there is no R_L:
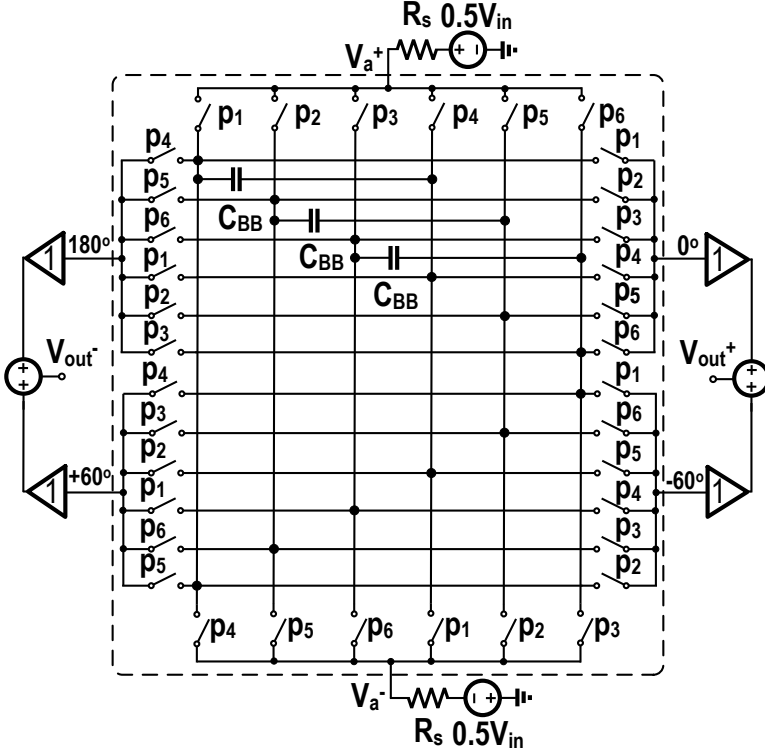
Figure 5.8: A proposed 6-path filter that achieves high stopband rejection and also eliminates the bandpass shapes located at $2kf_{\text{lo}}$ and $3kf_{\text{lo}}$, $k \in \mathbb{Z}$.

$$T(M\omega_{\text{lo}} + \Delta\omega) = \left(e^{-j\frac{M\pi}{3}} + 1\right) \frac{\text{sinc}^2\left(\frac{M\pi}{6}\right)}{6j(R_S + R_{SW})C_{BB}\Delta\omega + 1}. \tag{5.8}$$

Therefore, the transfer function of the filter for $0 \leq \omega \leq 4\omega_{\text{lo}}$ can be found by the addition of the transfer function of the filter (5.8) for $-4 \leq M \leq 4$ as described by:

$$T(\omega) = \sum_{m=-4}^{4} \left(e^{-j\frac{m\pi}{3}} + 1\right) \text{sinc}^2\left(\frac{m\pi}{6}\right) G(\omega - m\omega_{\text{lo}}) \tag{5.9}$$

where $G(\omega)$ is $1/[j6\,(R_S + R_{SW})\,C_{BB}\omega + 1]$. In the same manner, the transfer function of the filter at node V_{out1} and V_{out2} can be found by (5.10) and (5.11), respectively.

$$\frac{V_{\text{out1}}(\omega)}{V_{\text{in}}(\omega)} = \sum_{m=-4}^{4} \text{sinc}^2\left(\frac{m\pi}{6}\right) G(\omega - m\omega_{\text{lo}}) \tag{5.10}$$

$$\frac{V_{out2}(\omega)}{V_{in}(\omega)} = \sum_{m=-4}^{4} e^{-j\frac{m\pi}{3}} \text{sinc}^2\left(\frac{m\pi}{6}\right) G(\omega - m\omega_{lo}) \tag{5.11}$$

The simulated and calculated transfer function and phase of the filter at node V_{out1}, V_{out2} and V_{out} are shown in Fig. 5.7 for $f_{lo} = 1$ GHz, $R_S = 50\ \Omega$, $R_{SW} = 10\ \Omega$ and $C_{BB} = 50$ pF. It clearly shows the cancellation of the bandpass shapes of the filter around $3f_{lo}$. As can be seen, mathematical derivation (5.9) agrees well with simulation results.

It is possible to get rid off the bandpass shapes at even harmonics of the clock frequency f_{lo} by using a differential structure. If we make the circuit shown in Fig. 5.3(b) differential, the circuit illustrated in Fig. 5.8 results. The baseband capacitors C_{BB} are made differential to save area. The transfer function of the filter $(V_{out}^+ - V_{out}^-)/V_{in}$ for $M\omega_{lo} + \Delta\omega$ is:

$$T(M\omega_{lo} + \Delta\omega) = 0.5\left(1 - e^{-jM\pi}\right) \times \left(e^{-j\frac{M\pi}{3}} + 1\right) \times \frac{\text{sinc}^2\left(\frac{M\pi}{6}\right)}{6j(R_S + R_{SW})C_{BB}\Delta\omega + 1}. \tag{5.12}$$

The transfer function of the filter for $0 \leq \omega \leq 4\omega_{lo}$ can be found by the addition of the transfer function of the filter (5.12) for $-4 \leq M \leq 4$ as described by:

$$T(\omega) = \sum_{m=-4}^{4} \frac{1 - e^{-jm\pi}}{2}\left(e^{-j\frac{m\pi}{3}} + 1\right)\text{sinc}^2\left(\frac{m\pi}{N}\right)G(\omega - m\omega_{lo}) \tag{5.13}$$

where $G(\omega)$ is $1/[j6(R_S + R_{SW})C_{BB}\omega + 1]$. The simulated and calculated transfer function of the filter (Fig. 5.8) are shown in Fig. 5.9 for $f_{lo} = 1$ GHz, $R_S = 50\ \Omega$, $R_{SW} = 10\ \Omega$ and $C_{BB} = 50$ pF. It clearly shows the cancellation of the bandpass shapes of the filter around $2f_{lo}$ and $3f_{lo}$. As can be seen, mathematical derivation (5.13) agrees well with simulation results. According to (5.13), the third harmonic rejection of the filter is approximately:

$$HR3 \approx 12C_{BB}(R_S + R_{SW})\omega_{lo} \tag{5.14}$$

(5.14) is just the rejection provided by a BPF with $f_c = f_{lo}$ and bandwidth of $[1/(6\pi C_{BB}(R_{SW} + R_S)]$ at $f_{in} = 3f_{lo}$.[4] For $f_{lo} = 1$ GHz, $R_S = 50\ \Omega$, $R_{SW} = 10\ \Omega$ and $C_{BB} = 50$ pF, (5.14) shows HR3 = 47.1 dB which is in agreement with simulation results. Furthermore, the effect of 1% and 5% mismatch between the voltage gain of the amplifiers in Fig. 5.8 on the transfer function of the filter is illustrated in Fig. 5.9 which shows that 5% mismatch leads to a 7 dB reduction in the 3rd harmonic rejection of the filter.

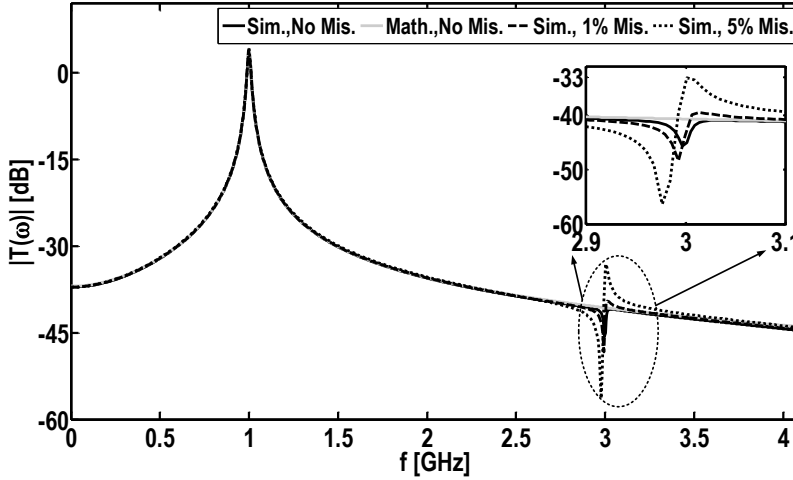[4]Therefore, reducing the center frequency of the filter, f_{lo}, lowers HR3 of the filter.

Figure 5.9: The simulated and calculated transfer function of the filter shown in Fig. 5.8 for $f_{lo} = 1$ GHz, $R_S = 50 \ \Omega$, $R_{SW} = 10 \ \Omega$ and $C_{BB} = 50$ pF. It also shows the effect of 1% and 5% mismatch in the voltage gain of the buffers in Fig. 5.8 on the transfer function of the filter.

5.3 Input-Matching and Amplification

To acquire low-noise input-matching and amplification for the filter, the buffers with voltage gain of 1 in Fig. 5.8 are replaced by voltage amplifiers with a voltage gain of A and two series RC impedances ($R_F - C_F$) are exploited to provide input-matching. Therefore the filter shown in Fig. 5.8 will be modified to a filter illustrated in Fig. 5.10(a). One of the issues of applying a feedback around an N-path filter is the fact that lots of up- and down- conversions occur in the circuit due to the inherent mixing behavior of the N-path filters and tracking all these conversions is a cumbersome task. In contrast, we will show that utilizing the proposed intuitive analysis method in section 5.2, eases the analysis of the modified filter shown in Fig. 5.10(a).

5.3.1 Input-Matching

At first, we will find the input impedance of the filter when the series capacitor in the feedback, C_F, is short-circuited and eventually its effect will be included. By using the technique mentioned in section 5.2, the single-ended LPF counterpart of the filter is found by substituting the switched-capacitor section with an equivalent baseband capacitance of $6C_{BB}$ as illustrated in Fig. 5.10(b). It should be noted that the extra phase-shift due to the second set of switches is embedded into the voltage gain of the amplifier. The effective impedance due to the Miller effect on R_F can be modeled by
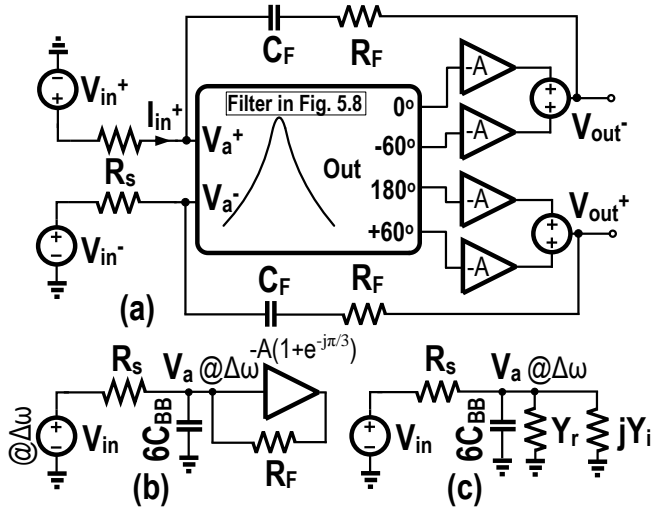
Figure 5.10: (a) A modification to the filter shown in Fig. 5.8 to provide input-matching and amplification (b) The single-ended LPF counterpart of the filter when f_{in} is around f_{lo} (c) Modeling the effect of the shunt-feedback resistor R_F with a complex admittance at the input port of the equivalent low-frequency counterpart of the filter when f_{in} is around f_{lo}.

a complex shunt admittance, $Y_r + jY_i$, as shown in Fig. 5.10(c) and described by (5.15).

$$Y_r + jY_i = \frac{1 + A(1 + e^{-j\pi/3})}{R_F} \tag{5.15}$$

where A is the voltage gain of the amplifiers in Fig. 5.10(a) and for now, we assume that they are ideal voltage amplifiers. (5.15) implies that:

$$\begin{aligned} Y_r &= \frac{1}{R_F}\left(1 + 1.5A\right) \\ Y_i &= -\frac{\sqrt{3}A}{2R_F}. \end{aligned} \tag{5.16}$$

The transfer function from $V_{in}(\Delta\omega)$ to $V_a(\Delta\omega)$ in Fig. 5.10(c) is:

$$D(\Delta\omega) = \frac{1}{1 + R_S Y_r + jR_S\left(6C_{BB}\Delta\omega + Y_i\right)} \tag{5.17}$$
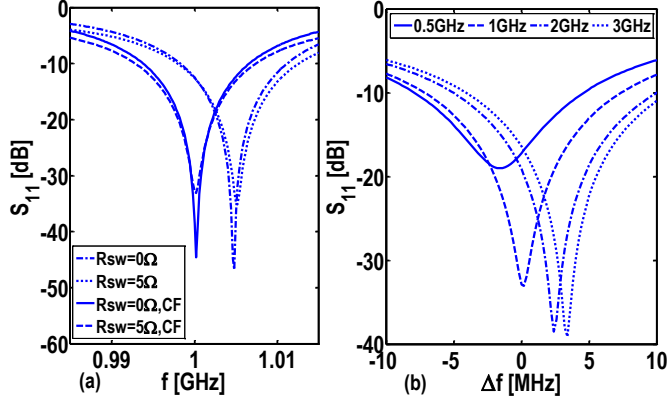
Figure 5.11: (a) The S_{11} of the filter with and without series capacitance $C_F = 280$ fF for $f_{lo} = 1$ GHz and two different values of the switch resistance, $R_{SW} = 0$ and 5 Ω (b) The S_{11} of the filter with series capacitance of $C_F = 280$ fF and switch resistance of $R_{SW} = 5$ Ω for different clock frequencies.

and therefore as we discussed in section 5.2, the transfer function from $V_{in}^+ (\omega_{lo} + \Delta\omega)$ to $V_a^+ (\omega_{lo} + \Delta\omega)$ is $H(\omega_{lo} + \Delta\omega) = \text{sinc}^2 \left(\frac{\pi}{6}\right) D(\Delta\omega)$. Therefore, the input impedance looking into node V_a^+ is found by (5.18).

$$Z_{in}(\omega_{lo} + \Delta\omega) = \frac{V_a^+(\omega_{lo} + \Delta\omega)}{I_{in}^+(\omega_{lo} + \Delta\omega)} = \frac{R_S V_a^+(\omega_{lo} + \Delta\omega)}{V_{in}^+(\omega_{lo} + \Delta\omega) - V_a^+(\omega_{lo} + \Delta\omega)} =$$
$$R_S \frac{H(\omega_{lo} + \Delta\omega)}{1 - H(\omega_{lo} + \Delta\omega)} = R_S \underbrace{\frac{\beta}{1 - \beta}}_{\text{Re}} || \frac{\beta}{Y_r} || j \underbrace{\frac{-\beta}{6C_{BB}\Delta\omega + Y_i}}_{\text{Im}} \tag{5.18}$$

where β is $\text{sinc}^2 \left(\frac{\pi}{6}\right)$. The required value of R_F to have $\text{Re}(Z_{in}) = R_S$ is:

$$R_F = R_S \times \frac{1 + 1.5A}{2\beta - 1}. \tag{5.19}$$

As can be deduced from (5.18), the frequency at which the input impedance is perfectly matched to the source impedance R_S is shifted upward with respect to the clock frequency due to the addition of the two phase-shifted paths (5.20).

$$\Delta f = \frac{-Y_i}{12\pi C_{BB}} = \frac{A}{8\pi\sqrt{3}R_F C_{BB}} \tag{5.20}$$

As an example, the required value of R_F for input-matching is 970 Ω for $R_S = 50$ Ω and $A = 10$. The offset frequency at which the input impedance is real, will be 4.7

MHz for $C_{BB} = 50$ pF. Fig. 5.11(a) plots the simulated S_{11} at clock frequency of 1 GHz for $R_{SW} = 0$ and 5 Ω which agrees well with our calculations (5.18). It is possible to eliminate the shift in the center frequency of the S_{11} by using a complex impedance (series RC) instead of a simple resistor as shown in Fig. 5.10(a). The extra phase-shift at the output port of the filter is around $-30°$. If we make the phase of the impedance used in the feedback equal to this phase-shift, it is possible to eliminate the frequency offset in the S_{11} of the filter. Therefore, we should have:

$$\text{angle}\left(R_F + \frac{1}{jC_F}\right) = -\frac{\pi}{6}. \tag{5.21}$$

Consequently, the required value of the series feedback capacitor C_F for this purpose is:

$$C_F = \frac{\sqrt{3}}{\omega_{lo}R_F}. \tag{5.22}$$

As an example, by using (5.22), the required value of C_F is 280 fF for a clock frequency of 1 GHz. The elimination of the offset frequency is clearly demonstrated in Fig. 5.11(a). Because the value of C_F depends on the clock frequency, the perfect cancellation of the frequency offset only happens for one clock frequency. This is illustrated in Fig. 5.11(b) as a function of offset frequency, Δf, from f_{lo} for different values of f_{lo}.

If we assume that the amplifiers used in the filter have a non-zero output impedance of r_o, the required value of R_F and C_F for input-matching are modified to:

$$R_F = R_S \frac{1 + 1.5A}{2\beta - 1} - 0.5r_o,$$
$$C_F = \frac{\sqrt{3}}{\omega_{lo}(R_F + 0.5r_o)}. \tag{5.23}$$

5.3.2   Transfer Function of the Modified Filter

By using the single-ended equivalent baseband circuit of the filter (see section 5.2) as depicted in Fig. 5.12(a), the transfer function of the filter at node V_{out} is:

$$G_m(\Delta\omega) = \frac{\gamma_m(0.5r_o - \alpha_m Z_{Fm})}{0.5r_o + Z_{Fm} + R_S(1 + \alpha_m) + 6j(Z_{Fm} + 0.5r_o)R_S C_{BB}\Delta\omega} \tag{5.24}$$

where α_m is $A\left(1 + e^{-jm\frac{\pi}{3}}\right)$, γ_m is $0.5\left(1 - e^{-jm\pi}\right)$ and Z_{Fm} is $R_F - j/(mC_F\omega_{lo})$. As discussed in section 5.2, the total transfer function of the filter for $0 \leq \omega \leq 4\omega_{lo}$ can be found by (5.25).
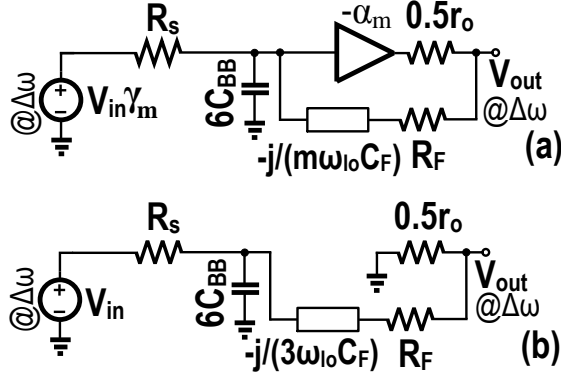
Figure 5.12: (a) The single-ended LPF counterpart of the filter when the input frequency is around mf_{lo} (b) The single-ended LPF counterpart of the filter when the input frequency is around $3f_{\text{lo}}$.

$$
\begin{aligned}
\text{T}(\omega) &= \sum_{m=-4}^{m=4} \text{sinc}^2\left(\frac{m\pi}{6}\right) \text{G}_m(\omega - m\omega_{\text{lo}}) = \\
&\text{sinc}^2\left(\frac{\pi}{6}\right)\left[\text{G}_1(\omega - \omega_{\text{lo}}) + \text{G}_{-1}(\omega + \omega_{\text{lo}})\right] + \\
&\text{sinc}^2\left(\frac{\pi}{2}\right)\left[\text{G}_3(\omega - 3\omega_{\text{lo}}) + \text{G}_{-3}(\omega + 3\omega_{\text{lo}})\right]
\end{aligned}
\tag{5.25}
$$

The LPF counterpart of the filter for input frequencies around $3f_{\text{lo}}$ is shown in Fig. 5.12(b). Interestingly, in this case (matched-input and non-zero r_{o}), the transfer function of this filter, $\text{G}_3(\Delta\omega)$, is not fully eliminated due to a residual feedforward path through Z_{F3} to node V_{out} as illustrated in Fig. 5.12(b). From (5.23) and (5.25), assuming that $|\alpha_1| \gg 1$ and $R_F \gg 0.5r_{\text{o}}$, it can be inferred that the 3rd harmonic rejection of the filter is:

$$
\frac{1}{\text{HR3}} \simeq \sqrt{\frac{\chi^2}{6.4} + \left(\frac{\beta}{6\text{C}_{\text{BB}}\text{R}_{\text{S}}\omega_{\text{lo}}}\right)^2 - \frac{1}{25}\frac{\beta\chi}{\text{C}_{\text{BB}}\text{R}_{\text{S}}\omega_{\text{lo}}}}
\tag{5.26}
$$

where

$$
\chi = \frac{(2\beta - 1)}{\text{A}^2} \times \frac{r_{\text{o}}}{\text{R}_{\text{S}}} \times \text{sinc}^2\left(\frac{\pi}{2}\right).
\tag{5.27}
$$

In the case of $r_{\text{o}} = 0\ \Omega$, (5.26) will be simplified to:

$$\text{HR3} \simeq \frac{12\text{C}_{\text{BB}}\text{R}_\text{S}\omega_{\text{lo}}}{2\beta}. \tag{5.28}$$

(5.28) is $1/(2\beta)$ times smaller than (5.14) due to the input-matching. This is due to the fact that the filter is not input-matched at $3f_{\text{lo}}$ due to the signal cancellation at this frequency.

5.3.3 Stability of the Filter

It can be shown that the differential loop-gain of the filter at f_{lo} is:

$$\text{A}_{\text{loop}} = \beta \times \left| \frac{\text{R}_\text{S}}{\text{R}_\text{S} + \text{Z}_{\text{F1}} + 0.5r_{\text{o}}} \times \alpha_1 \right|. \tag{5.29}$$

By substituting Z_{F1} into (5.29) and assuming that $\text{A} \gg 2\beta$ and $\text{A} \gg 1$, (5.29) can be simplified to:

$$\text{A}_{\text{loop}} \approx \beta(2\beta - 1) \tag{5.30}$$

which is < 1 and for frequencies far from f_{lo}, the loop-gain of the filter will be much lower due to the provided bandpass filtering. Moreover, it can be shown that the common-mode loop-gain of the filter is zero.

5.4 Circuit Simulations in CMOS 28 nm FDSOI

To demonstrate the feasibility of the introduced technique, Fig. 5.13(a) presents a possible transistor level implementation of the filter. The amplifiers used in the filter are realized by G_m cells having a transconductance of g_m, an output impedance of r_o and therefore an intrinsic voltage-gain of $\text{A}_0 = g_\text{m}r_o$. Also, two cross-coupled G_m cells with a value of g_mn are added to double the voltage gain of the filter (Fig. 5.13(a)). In this case, r_o and A in (5.23)-(5.27) should be substituted by

$$\begin{aligned}
r'_\text{o} &= \frac{\text{A}_0}{g_\text{m} - 0.5g_\text{mn}\text{A}_0}, \\
\text{A} &= \frac{\text{A}_0}{2 - \dfrac{g_\text{mn}}{g_\text{m}}\text{A}_0}.
\end{aligned} \tag{5.31}$$

Switches are made of NMOS transistors with a size of 65um/0.03um to achieve an on-resistance of $5\,\Omega$. The bulk and source of each switching transistor are tied together
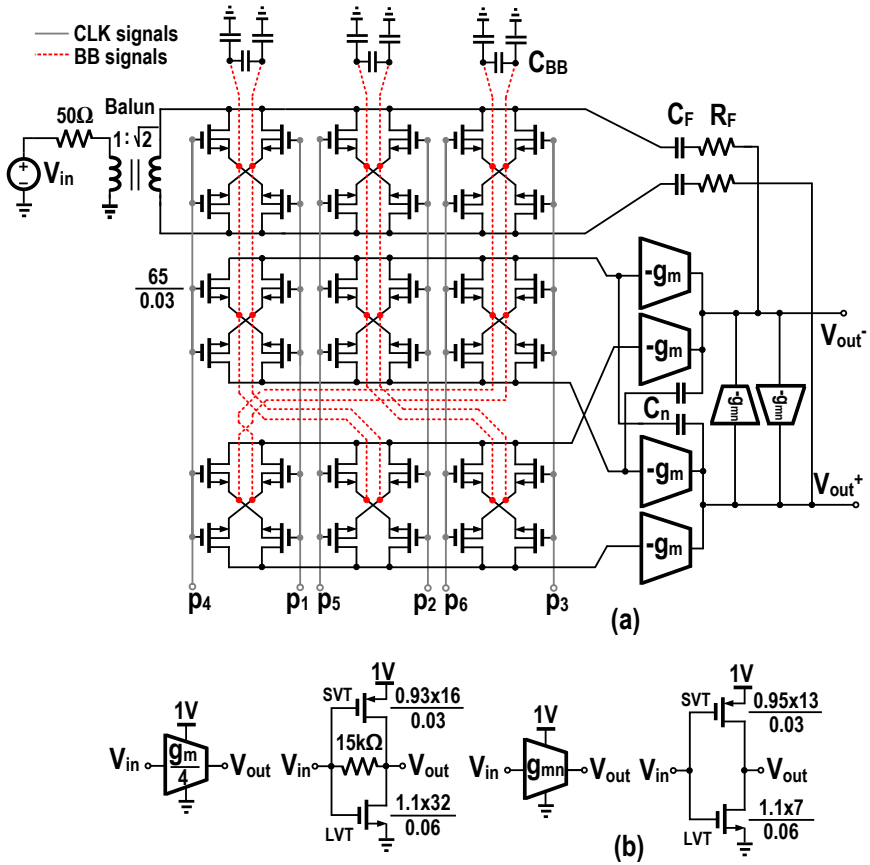
Figure 5.13: (a) Transistor level schematic of the filter (b) Realization of amplifiers and negative resistors using self-biased inverters

to avoid an increase in the threshold voltage of the transistor. All the capacitors are made of Metal-Oxide-Metal (MOM) capacitors. Some single-ended capacitors are also added to enhance the common-mode rejection of the filter. Implementation of the amplifiers and negative resistors using self-biased inverters is shown in Fig. 5.13(b). The intrinsic gain of the self-biased inverters is about 10 and the g_m/I_{dc} of them is 24.5. The noise figure of the filter is calculated in Appendix A. A value of 65 mS is chosen for g_m for NF considerations. Without any negative resistance, the NF is 2.55 dB according to (5.32). It was possible to double the voltage gain of the amplifier by doubling its output resistance, r_o', using the two negative G_m cells. These have noise of their own, but this is compensated by the fact that the required shunt-feedback

Figure 5.14: (a) The simulated S_{11} of the filter at $f_{lo} + \Delta f$ without utilizing the nulling capacitance C_n for different clock frequencies (b) The S_{11} of the filter at $f_{lo} + \Delta f$ with utilizing the nulling capacitance C_n for different clock frequencies.

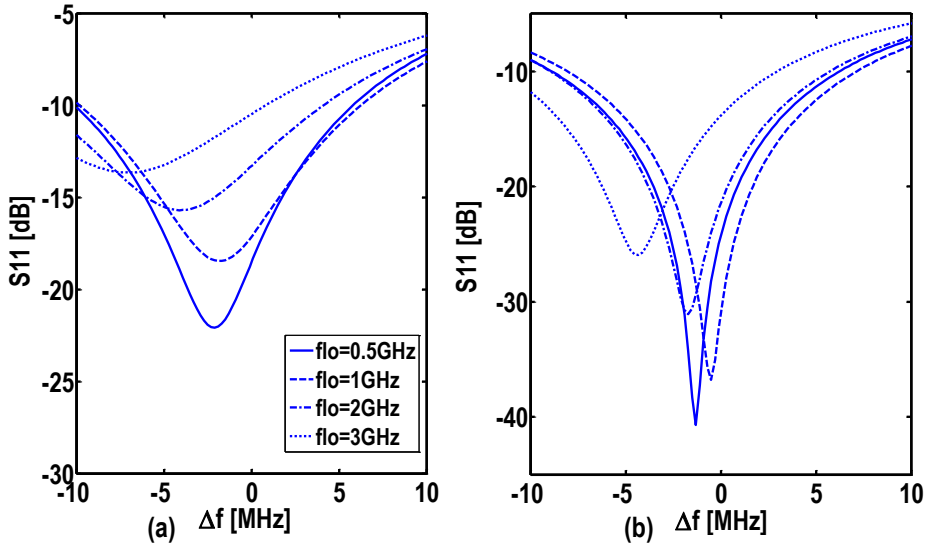resistance R_F for input matching increases which lowers the noise contribution of R_F.[5] In fact, by choosing a g_{mn} of 6.5 mS, the NF of the filter reduces by 0.2 dB. The total power consumption of all amplifiers is 10.6 mW and the power consumption of the negative resistors is 0.6 mW. Therefore, the total analog power consumption of the filter is 11.2 mW. A modulo-6 ring counter [108] is used to obtain 6 non-overlapping clock signals with duty cycle of 1/6 and a power consumption of 14 mW/GHz.[6]

5.4.1   The effect of Parasitic Capacitance on the Filter

The effect of parasitic capacitance on the performance of N-path filters has not been addressed in literature. Although it is possible to utilize the method introduced in [101], it requires exhaustive and lengthy calculations and does not provide us with closed-form formulas. In Appendix B, through a simple method, the effect of parasitic capacitance on the transfer function of an N-path filter around f_{lo} is explored. In section 5.2, the effect of the baseband current due to the baseband voltage was modeled by two shunt resistances $N(R_S + R_{sw})$ and $N(R_L + R_{sw})$. These shunt resistors can be interpreted as the effective impedance seen by each baseband capacitor. In the same manner, in Appendix B, it is shown that the effect of parasitic capacitance

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[5]It can be shown by (5.23) and (5.31) that $dR_F/dg_{mn} > 0$ if $g_m > (2\beta - 1)/(1.5R_S)$.

[6]Without layout parasitics.

Figure 5.15: (a) The simulated transfer function of the filter in a large frequency range for different clock frequencies (b) The simulated NF of the filter for different clock frequencies (c) The simulated IIP$_3$ of the filter for different offset frequencies, Δf.

on N-path filters can be modeled by a parallel complex admittance to the baseband capacitors.

In this way, the method introduced in section 5.2 can be utilized to calculate the effect of parasitic capacitors on the transfer function of the filter. The real part of this admittance introduces loss and also reduces the input impedance and hence leads to a degradation in the S$_{11}$ and NF of the filter. Its imaginary part reduces the center frequency of the N-path filter. This can be compensated by lowering the phase of the feedback impedance. Therefore, the value of C$_F$ is modified from 280 fF to 500 fF. The input capacitances of the four g_ms and parasitic capacitance of switches introduce about 2 dB of loss and a degradation in the S$_{11}$ of the filter. To partly compensate

111

Table 5.1: The Values of Different components Used in the Circuit Simulations

g_m [mS]	g_{mn} [mS]	R_{SW} [Ω]	R_F [Ω]	C_F [fF]	C_{BB} [pF]
65	6.5	5	820	500	50

Table 5.2: Summary of Simulation Results

Gain [dB]	+26
NF [dB]	$2.5 - 3.4$
Frequency Band [GHz]	0.5-3
3rd Harmonic Rejection [dB]	40
IIP3$_{IB}$ [dBm]	-11
IIP3$_{OOB}$ [dBm] (Δf= +50MHz)	$+7$
IIP3$_{OOB}$ [dBm] (Δf= +100MHz)	$+16$
IIP3$_{OOB}$ [dBm] (Δf= +200MHz)	$+25$
BW [MHz]	40
S$_{11}$ [dB]	< -10
Supply Voltage [V]	1
P$_{analog}$ [mW]	11.2
P$_{digital}$ [mW/GHz]	14
CMOS Technology [nm]	28 FDSOI

that, two nulling capacitors C_n with a value of 60 fF are exploited as shown in Fig. 5.13(a). The simulated S$_{11}$ of the filter at different clock frequencies with and without the nulling capacitance C_n is illustrated in Fig. 5.14 which shows that using C_n, in principle, can improve the S$_{11}$ of the filter.

5.4.2 Transfer Function, NF and IIP$_3$ Simulations

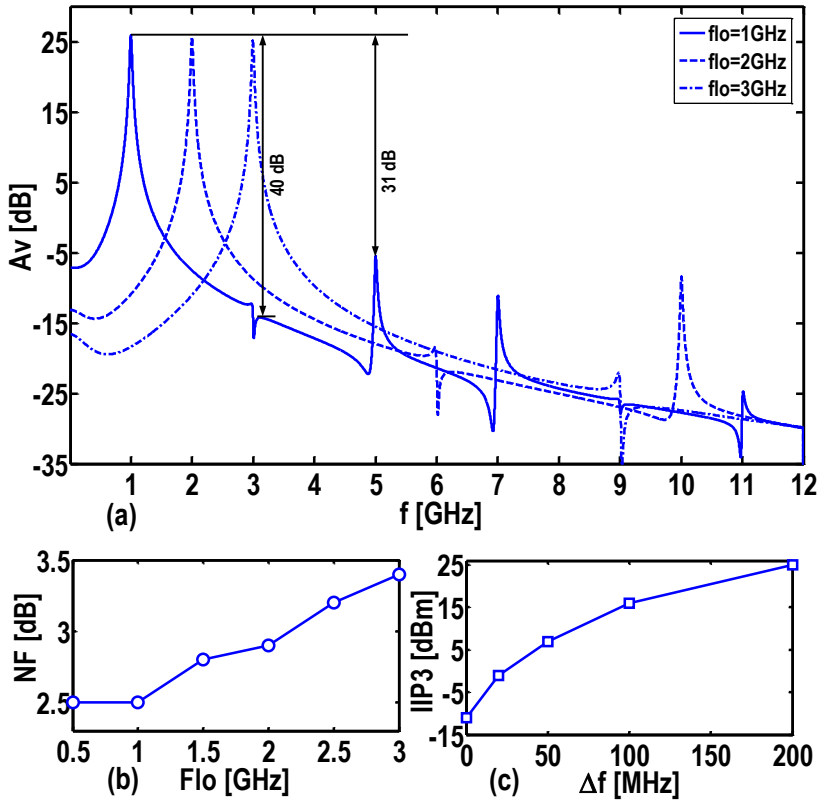Table 5.1 shows the values of different components that have been utilized in the filter design. The simulated transfer function of the filter in a large frequency range for different clock frequencies is illustrated in Fig. 5.15(a). As can be seen, the filter achieves a 3rd harmonic rejection of 40 dB. This is in agreement with our calculations in (5.26) which is 39.6 dB.[7] The simulated noise figure of the filter for different clock frequencies is shown in Fig. 5.15(b). The NF changes from 2.5 dB at $f_{lo} = 1$ GHz to 3.4 dB at $f_{lo} = 3$ GHz. The increase in the NF is because of the fact that the introduced loss due to the parasitic capacitances on the N-path filter exacerbates as

---

[7]According to (5.28), in the case of $r_{out} = 0$ Ω, 3rd harmonic rejection will be 40.2 dB. This means that the contribution of the residual path due to the feedback impedance is not important, in our case.
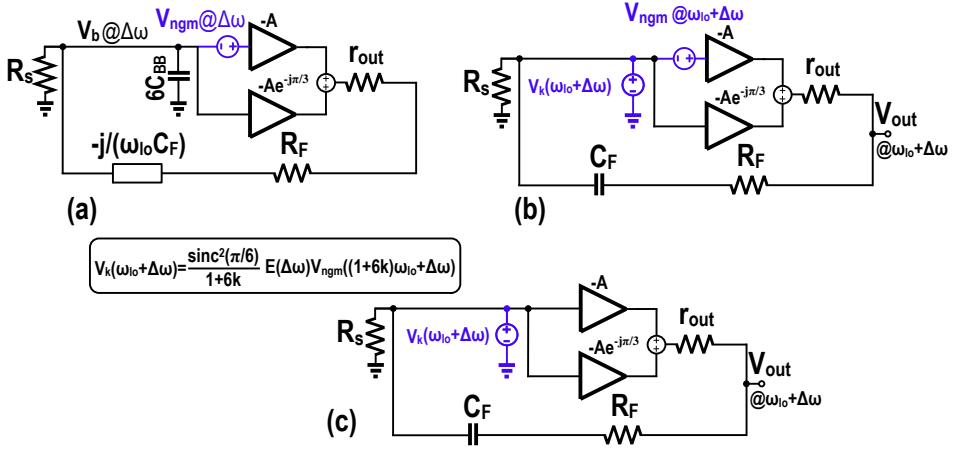
Figure 5.16: A method to find the transfer function of $V_{ngm}((1 + 6k)\omega_{lo} + \Delta\omega)$ to $V_{out}(\omega_{lo} + \Delta\omega)$: (a) The equivalent single-ended LPF counterpart of the filter to calculate $E(\Delta\omega) = V_b(\Delta\omega)/V_{ngm}(\Delta\omega)$ (b) A circuit to find the transfer function of $V_{ngm}(\omega_{lo} + \Delta\omega)$ to $V_{out}(\omega_{lo} + \Delta\omega)$ (c) A circuit to calculate the transfer function of $V_{ngm}((1 + 6k)\omega_{lo} + \Delta\omega)$ to $V_{out}(\omega_{lo} + \Delta\omega)$, $k \neq 0$.

the clock frequency increases (see Appendix B). In our case, the gain of the 6-path filter at $f_{lo} = 3$ GHz is 1 dB lower than the gain of the filter at $f_{lo} = 1$ GHz.

Fig. 5.15(c) plots the linearity performance of the filter. For IIP$_3$ simulations, two tones which are located at $f_{lo} + \Delta f + f_1$ and $f_{lo} + 2\Delta f + f_2$ have been used. f_{lo}, f_1 and f_2 are 1 GHz, 2 MHz and 3 MHz, respectively. As can be seen, the IIP$_3$ of the filter changes from -11 dBm (in-band) to $+25$ dBm (out-of-band) for $\Delta f = +200$ MHz.[8] The linearity of the filter is mostly limited by the G_m cells. Finally, a summary of simulation results is shown in Table 5.2.

5.5 Conclusions

One of the issues of N-path filters, which is the repetition of the bandpass shapes at higher harmonics of the clock frequency, is addressed. A technique to concurrently eliminate the bandpass shapes at second and third harmonics of a 6-path filter and a technique to provide input-matching for this filter, are proposed. Also, a simple way to calculate the transfer function of N-path filters over a large frequency range is presented. Moreover, a simple and intuitive method to find the effect of parasitic capacitance on the transfer function of N-path filters is shown. To demonstrate the

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[8]Note that the BW of the filter is 40 MHz.

feasibility of the proposed technique, a possible implementation of the filter in CMOS 28 nm FDSOI is demonstrated which shows the possibility of achieving a 40 dB of 3rd harmonic rejection.

5.A NF of the Filter

In this section, we calculate the NF of the filter shown in Fig. 5.13(a). In N-path filters, input signals located at $|1 + kN|f_{\text{lo}}$, $k \in \mathbb{Z}$ are downconverted to f_{lo} [19, 98, 101, 102]. In this case, signals located at $(1 + kN)f_{\text{lo}}$ are downconverted to baseband signals by the mixing operation of the first set of switches with gain of $N|a_{-(1+kN)}|$ and then these downconverted signals are upconverted to f_{lo} by the mixing operation of the second set of switches with gain of $N|a_1|$. Therefore, the voltage gain of signals located at $(1 + kN)f_{\text{lo}}$ to the output of the filter at f_{lo} is the transfer function of the LPF counterpart of the N-path filter that it is scaled by $N^2|a_{-(1+kN)}a_1|$. This can be simplified to $\text{sinc}^2\left(\frac{\pi}{N}\right)/(1 + kN)$.

Therefore, to find the noise figure of the filter, first we should find the transfer function of each noise source, V_{ni}, at $f_{\text{in}} = (1+kN)f_{\text{lo}}$ to the output voltage at $f_{\text{out}} = f_{\text{lo}}$. Based on what has been discussed in section 5.2, the LPF counterpart of the filter is made by substituting the switched-capacitor section with an equivalent baseband capacitance of NC_{BB}. Then, the baseband transfer function from the noise source to the voltage of the capacitor should be found $E_i(\Delta\omega) = V_b(\Delta\omega)/V_{ni}(\Delta\omega)$. Afterwards, we substitute the capacitor with a voltage source of $\text{sinc}^2\left(\frac{\pi}{N}\right)/(1+kN)E_i(\Delta\omega)V_{ni}((1+Nk)\omega_{\text{lo}}+\Delta\omega)$. Finally, $V_{\text{out}}(\omega_{\text{lo}})/V_n((1+kN)\omega_{\text{lo}})$ can be found by superposition. This procedure is illustrated in Fig. 5.16 for the input-referred noise of one of the G_m cells. The transfer function of other noise sources in the filter to the output of the filter can be found in the same way. It can be shown that the NF of the filter at its center frequency is approximately:

$$
F = \frac{1}{\beta}\left(1 + \frac{R_S R_F}{|0.5r_o' + Z_{F1}|^2} + \frac{R_{SW}}{R_S}\left|1 + \frac{R_S}{0.5r_o' + Z_{F1}}\right|^2\right) + \frac{A^2}{\beta}\left(\frac{2R_{SW}}{R_S} + \frac{2}{R_S g_m} + \frac{g_{mn}}{R_S g_m^2}\right)
$$

$$
\times \left(\frac{(1-\beta)R_S^2}{|0.5r_o' + Z_{F1}|^2} + \frac{\left|Z_{F1} + R_S\left[\beta + (1+\alpha_1)(1-\beta)\dfrac{Z_{F1}}{0.5r_o' + Z_{F1}}\right]\right|^2}{\beta|\alpha_1 Z_{F1} - 0.5r_o'|^2}\right).
$$

$$(5.32)$$

5.B The Effect of Parasitic Capacitance on N-path Filters

Here, through a simple method, the effect of parasitic capacitance on the transfer function of an N-path filter around f_{lo} is explored (Fig. 5.17(a)). First, we will find the effective impedance seen by each baseband capacitor in the presence of a source and a load parasitic capacitance, C_S and C_L, as shown in Fig. 5.17(b). As already mentioned in section 5.2, in the case of no parasitic capacitance, the effective impedance seen by each baseband capacitor is $N(R_S||R_L)$. Therefore, it is only needed to find the extra baseband current due to the two parasitic capacitances, C_P and C_L. For input frequencies around f_{lo}, each baseband voltage of the N-path filter can be described in the form of $V_{bi} = V_b e^{j(i-1)2\pi/N}$, $i = [1, N]$.[9] As illustrated in Fig. 5.17(b), the extra baseband current due to the two parasitic capacitances is found using the fact that C_S and C_L are charged from $V_b e^{-j2\pi/N}$ to V_b. Therefore we have

$$
\begin{aligned}
I_{bb}|_{Cs,CL} = \frac{\Delta Q}{T_{lo}} &= (C_S + C_L)f_{lo}V_b \left(1 - e^{-j2\pi/N}\right) \\
&= (C_S + C_L)f_{lo}V_b \left[2\sin^2\left(\frac{\pi}{N}\right) + j\sin\left(\frac{2\pi}{N}\right)\right].
\end{aligned}
\tag{5.33}
$$

Consequently, using (5.33), the effective admittance seen by each baseband node due to the parasitic capacitance is $1/R_P + jB_P$ which is described by (5.34).

$$
\begin{aligned}
\frac{1}{R_P} &= 2(C_S + C_L)f_{lo}\sin^2\left(\frac{\pi}{N}\right) \\
B_P &= (C_S + C_L)f_{lo}\sin\left(\frac{2\pi}{N}\right)
\end{aligned}
\tag{5.34}
$$

By exploiting the same technique used in section 5.2, the equivalent low-frequency counterpart of the filter shown in Fig. 5.17(c) will result. The finite value of R_P is responsible for the loss introduced by the parasitic capacitances and jB_S causes a reduction in the center frequency of the filter. Using Fig. 5.17(c), the transfer function of the LPF counterpart of the filter is

$$
G_p(\Delta\omega) = \frac{G_0}{j\left[C_{BB}\Delta\omega + C_p f_{lo}\sin\left(\frac{2\pi}{N}\right)\right]NG_0R_S + 1}
\tag{5.35}
$$

where G_0 is:

---

[9]In other words, the baseband voltages have the same magnitude but with different phase-shifts.
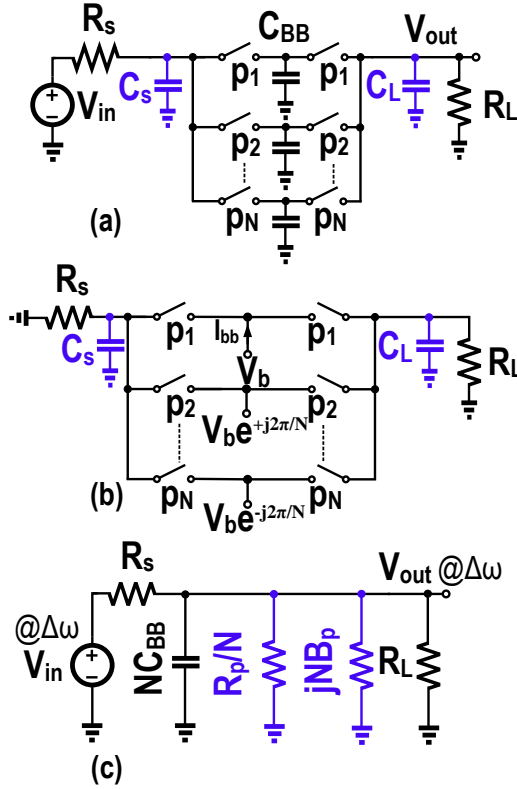
Figure 5.17: (a) An N-path filter with a second set of switches and parasitic capacitance at its input and output ports (b) An intuitive method to find the effective impedance seen by each baseband capacitor (c) The low-frequency counterpart of the N-path filter.

$$G_0 = \frac{R_L}{R_L + R_S} \times \frac{1}{1 + 2N(R_S||R_L)C_P f_{lo}\sin^2\left(\frac{\pi}{N}\right)}. \tag{5.36}$$

and $C_P = C_S + C_L$. Subsequently, the total transfer function of the filter is:

$$T(\omega_{lo} + \Delta\omega) = \text{sinc}^2\left(\frac{\pi}{N}\right) G_P(\Delta\omega). \tag{5.37}$$

In general, the parasitic capacitance: 1) reduces the center frequency of the filter by $C_P f_{lo}\sin\left(\frac{2\pi}{N}\right)/(2\pi C_{BB})$; 2) reduces the gain of the filter; and 3) due to the reduction of the effective resistance seen by the baseband capacitors, it increases the bandwidth of the filter or equivalently reduces the Q-factor of the filter.

Figure 5.18: (a) Taking into account the effect of the switch resistance on the effective impedance seen by each baseband capacitor (b) The resistive dividers due to the switch resistance, source and load resistance make transformers that effectively reduce the effect of the input and output parasitic capacitance on the transfer function of the filter (c) The low-frequency counterpart of the N-path filter.
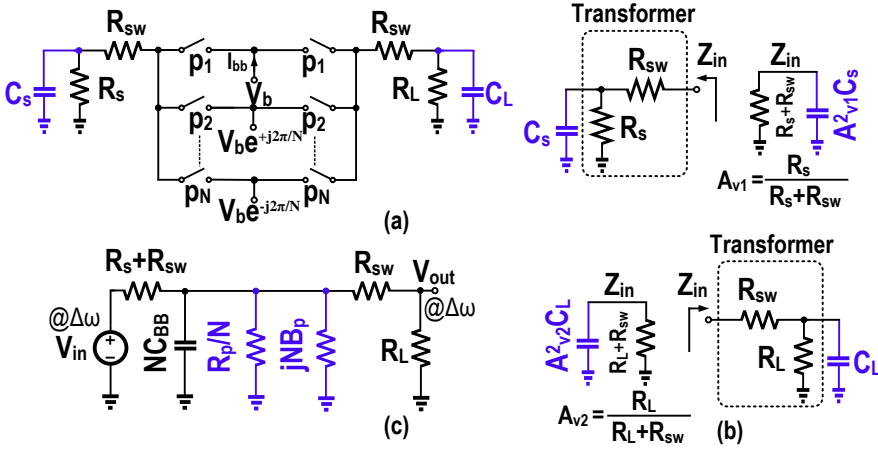
Finally, we want to include the effect of the switch resistance as well, such that our calculation accounts for both parasitic capacitance and switch resistance. Now, we investigate the effect of the switch resistance on the effective impedance seen by each baseband capacitor (Fig. 5.18(a)). First, we assume that $N(R_S||R_{SW})C_S \ll T_{lo}$ and $N(R_L||R_{SW})C_L \ll T_{lo}$ which means that the parasitic capacitances are charged completely within one clock cycle. Then, we make a crucial observation here. The two resistive dividers comprising the source resistance R_S and the switch resistance R_{SW} and also the load resistance R_L and the switch resistance R_{SW}, form an impedance transformer as shown in Fig. 5.18(b). Because the gain of the resistive dividers are $R_S/(R_S+R_{SW})$ and $R_L/(R_L+R_{SW})$, the effective capacitance seen at the input and the output port of the N-path filter are $C_S\left[R_S/(R_S+R_{SW})\right]^2$ and $C_L\left[R_L/(R_L+R_{SW})\right]^2$, respectively. Therefore, the modified values of $1/R_P$ and B_P are found by substituting C_S and C_L in (5.34) with $C_S\left[R_S/(R_S+R_{SW})\right]^2$ and $C_L\left[R_L/(R_L+R_{SW})\right]^2$, respectively.

Afterwards, the transfer function of the filter around f_{lo} can be found by scaling , $\text{sinc}^2\left(\frac{\pi}{N}\right)$, and transforming the transfer function of the LPF counterpart of the filter shown in Fig. 5.18(c) to around f_{lo}.

$$T(\omega_{lo} + \Delta\omega) = \text{sinc}^2\left(\frac{\pi}{N}\right) G_p(\Delta\omega) \tag{5.38}$$
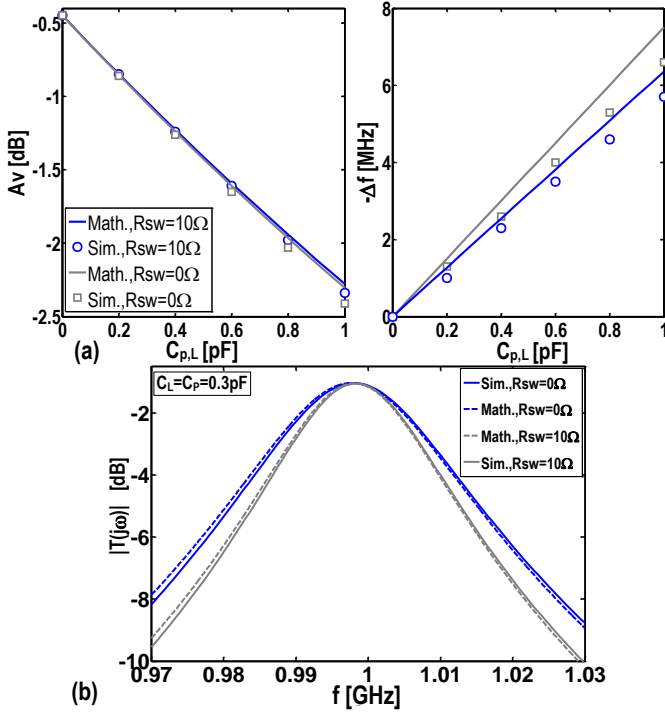
Figure 5.19: (a) A comparison between simulated and calculated voltage gain A_v, shift in the center frequency of the filter Δf for $C_{BB} = 30$ pF, $R_S = 50$ Ω, $f_{lo} = 1$ GHz, N = 8 and $R_{SW} = 0$ and 10 Ω for different values of load and source capacitance, $C_L = C_S$ (b) Comparing the simulated and calculated transfer function of the filter for a source and a load capacitance of 0.3 pF for $R_{SW} = 0$ and 10 Ω.

where

$$G_p(\Delta\omega) = \frac{R_L}{R_L + R_{SW}} \frac{G_0}{j(C_{BB}\Delta\omega + B_P)NG_0(R_S + R_{SW}) + 1} \qquad (5.39)$$

$$G_0 = \frac{1}{1 + \dfrac{R_S + R_{SW}}{R_L + R_{SW}} + (R_S + R_{SW})\dfrac{N}{R_P}}. \qquad (5.40)$$

In the case of no load resistance, the simulation results and mathematical derivations of the effect of parasitic capacitance at both the input and output port of the filter, $C_S = C_L$, is illustrated in Fig. 5.19(a). As can be seen in this case, the gain of the filter to a first order, is independent of the switch resistance. This is because in

the case of no load resistance, as R_{SW} increases, the effect of C_S on the gain of the filter decreases while the effect of C_L increases. The simulated transfer function of the filter for a source and a load capacitance of 0.3 pF is compared with its mathematical derivation (5.38) for two different values of the switch resistance, 0 and 10 Ω, and no load resistance in Fig. 5.19(b).

Chapter 6

Conclusions

6.1 Summary and Conclusions

In chapter 1, a motivation towards multi-band multi-mode RF transceivers was given. Moreover, it was shown that having an integrated tunable BPF is a must to reduce the cost and form-factor of multi-standard receivers.

In chapter 2, a summary of different approaches to the integration of RF BPFs was given. Furthermore, It was illustrated that there are tight tradeoffs among the center frequency, Q-factor, power consumption and DR of G_m-C BPF. Q-enhanced LC BPFs suffer from a limited DR due to the limited Q-factor of on-chip inductors. On the other hand, N-path filters can decouple the required Q-factor from the DR of the filter. N-path filters can provide us with high-Q BPF where its center frequency can be changed by a mere change of its clock frequency. Because the main constituents of N-path filters are switches and capacitors, it is compatible with submicron CMOS technology and benefits from process scaling. These reasons have motivated us to explore the design and implementation of high-order center-frequency tunable BPFs based on N-path filtering.

In chapter 3, a widely tunable 4th order BPF based on the subtraction of two 2nd order 4-path filters with slightly different center frequencies was proposed. The center frequency of each 4-path filter was slightly shifted relative to its clock frequency (one upward and the other one downward) by a G_m-C technique. Capacitive splitting of the input signal was used to reduce the mutual loading of the two 4-path BPFs and increase their Q-factors. The filter was tunable from 0.4 GHz to 1.2 GHz with approximately constant bandwidth of 21 MHz. The in-band 1-dB compression point of the filter is -4.4 dBm, while the in-band IIP3 of the filter was $+9$ dBm and the out-of-band IIP3 is $+29$ dBm ($\Delta f = 50$ MHz). The stopband rejection of the filter was 55 dB and the NF of the filter was 10 dB. The static and dynamic current

consumption of the filter were 2.8 mA from 2.5 V and 12 mA from 1.2 V, respectively (at 1 GHz). The LO leakage power to the input port was < -60 dBm. The filter has been fabricated in CMOS LP 65 nm technology and the active area was 0.127 mm^2.

In chapter 4, a widely-tunable and highly-selective filter with a decent amount of embedded amplification was introduced. In this way, while the blockers are eliminated by filtering, the passband gain of the filter relaxes the noise requirement of the following stages in the receiver. Furthermore, a design methodology for synthesis of active N-path BPF was introduced. Based on this methodology, a 0.1-to-1.2 GHz tunable 6th-order N-path channel-select filter in 65 nm LP CMOS technology was proposed. It was based on coupling N-path filters with gyrators, achieving a "flat" passband shape and high out-of-band linearity. A Miller compensation method was utilized to considerably improve the passband shape of the filter. The bandwidth of the filter was around 8 MHz which was equivalent to having a Q-factor of 125 at $f_{\mathrm{lo}} = 1$ GHz. The filter had 2.8 dB NF, $+25$ dB gain, $+26$ dBm wideband IIP3 ($\Delta f = 50$ MHz), an out-of-band 1dB blocker compression point $B_{1\mathrm{dB,CP}}$ of $+7$ dBm ($\Delta f = 50$ MHz) and 59 dB stopband rejection. The analog and digital part of the filter drew 11.7 mA and $3 - 36$ mA from 1.2 V, respectively. The LO leakage to the input port of the filter was < -64 dBm at a clock frequency of 1 GHz. The proposed filter only consisted of inverters, switches and capacitors and therefore it is friendly with process scaling. The active area of the filter was 0.27 mm^2.

In chapter 5, a technique to concurrently eliminate the bandpass shapes at second and third harmonics of a 6-path filter was proposed. In conventional N-path filters, blockers located at second and third harmonics of the clock frequency are passed with less attenuation when the number of phases is higher which potentially can degrade the sensitivity of a receiver that comes after it. Moreover, a compact method to calculate the transfer function of N-path filters over a large frequency range was introduced which avoided the lengthy analysis presented in literature so far. Furthermore, through a simple and intuitive method, the effect of parasitic capacitance on the transfer function of N-path filters was explored. Predictions agreed well with simulation results. To demonstrate the feasibility of the proposed technique, the simulation results of a possible implementation of the filter in CMOS 28 nm FDSOI were illustrated, showing the possibility of achieving a 40 dB of 3$^{\mathrm{rd}}$ harmonic rejection, good out-of-band linearity and a decent amount of gain.

6.2 Original Contributions

- A subtraction of the transfer functions of two 2$^{\mathrm{nd}}$ order N-path filters with slightly different center frequencies as a method to obtain a 4$^{\mathrm{th}}$ order tunable BPF and to eliminate the effect of the switch resistance on the stopband rejec-

tion of the filter. (chapter 3)

- A G_m-C technique to shift the center frequency of the N-path filters upward and downward with respect to f_{lo}. (chapter 3)

- Exploitation of a second set of switches in conventional N-path filters to eliminate the effect of switch resistance on the ultimate rejection of the filter. (chapter 3 and 5)

- Introducing a simple and intuitive way of analyzing N-path filters. (chapter 4 and 5)

- A concept and design methodology of high-order active N-path filters. (chapter 4)

- Concurrent elimination of the bandpass shapes of a 6-path filter at second and third harmonics of f_{lo}. (chapter 5)

- Introducing a simple and intuitive way of analyzing the effect of parasitic capacitors on N-path filters. (chapter 5)

6.3 Future Work

Tremendous improvement in the raw speed of transistors and the availability of high-density capacitors in CMOS technology have made possible the integration of RF frequency N-path filters. These filters are quite interesting in a sense that they provide us with integrated BPFs with high selectivity, wide-range center frequency tunability and high dynamic range. However, to be more than an academic curiosity and to be truly exploitable in industry, some remaining limitations and issues need to be addressed and resolved. In below, some suggestions for future work are given.

- There is an enormous urge towards multi-standard, multi-mode transceivers. The technique of subtracting the transfer function of two 2nd order BPFs with slightly different center frequencies to obtain a 4th BPF (chapter 3) can be extended to achieve a tunable higher-order BPF. In fact, simulations show that it is possible to achieve an $2n^{th}$ order BPF by subtracting the transfer function of n 2nd order BPFs with slightly different center frequencies [i.e.,$\sum_{i=0}^{n}(-1)^i H_i(s)$]. This provides us with a great flexibility in choosing the desired bandwidth, rejection, and the center frequency of the resultant BPF.

- The proposed concept of active N-path filters (chapter 4) has lots of unexplored opportunities. These filters can potentially be an integrated substitution of SAW filters utilized in the receivers. Different filter topologies can be employed,

e.g. with higher-orders or having transmission zeros. One of the issues of active
N-path filters is the effect of parasitic capacitance on the passband shape of
the filter. We have demonstrated that parasitic capacitors introduce a loss
and an excess phase-shift into the N-path filter which leads to a distortion
in the passband shape of the filter. A Miller compensation method that was
proposed in chapter 4, is not applicable to other filter topologies.[1] Therefore,
some further research is necessary in elimination of the effect of the parasitic
capacitance in different filter architectures. In chapter 5, we showed that the
effect of parasitic capacitor can be modeled by a complex shunt admittance
in parallel with baseband capacitors of N-path filters where its real part is
responsible for the loss and its imaginary part is the cause of an excess phase-
shift. As shown in chapter 5, the loss and the excess phase-shift are functions
of the clock frequency. These should be considered in developing compensation
methods.

- FBAR resonators have high Q-factors and can operate at GHz range frequencies.
  A lattice-based high-order BPF based on FBAR resonators has been demon-
  strated with low insertion-loss in GHz range [53]. One of the issues associated
  with FBARs is that they are not tunable.[2] Also, one of the issues of N-path
  filters is the generation of low duty-cycle high-frequency clock signals with very
  low rise- and fall- time. This limits the frequency range of N-path filters. There
  is a possibility of combining FBAR filters with N-path filters. In this manner,
  1) the non-tunability of FBAR filters can be resolved and 2) we can achieve
  N-path filters with high-frequency capability. As an example, an N-path filter
  with clock frequency of f_{lo} where its baseband capacitors are substituted by
  bandpass impedances with center frequency of f_{res}, will result in a BPF with
  two main bandpass shapes at $f_{lo} + f_{res}$ and $f_{lo} - f_{res}$ provided that $f_{lo} > f_{res}$.
  This might be a good direction to be explored.

- The LO generation is one of the biggest challenges in N-path filters that needs
  to be explored. In SAW-based receivers, the out-of-band phase-noise of the
  LO signal is determined by knowing that the SAW filter already attenuates the
  out-of-band blocker to a level similar to the in-band interferers (i.e., more than
  20 dB of attenuation). However, in SAW-less receivers where an N-path filter
  is exploited as an RF filter, the situation is different. The available out-of-
  band blocker reaches to the input port of the N-path filter without any prior
  attenuation and can corrupt the desired signal due to the reciprocal mixing
  in N-path filters.[3] In this case, this 20 dB must be supplied by lowering the

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[1] The proposed technique works in cases where the filter is *unilateral*.

[2] Of course, in some cases, it can be seen as a benefit.

[3] An N-path filter is just a passive-mixer.

phase noise of the LO signal by the same amount (20 dB) to achieve a reciprocal-mixing performance similar to SAW-based receivers. This leads to a considerable increase in the power consumption of the LO generation circuitry. [102] has presented the mathematical derivation of the effect of the phase-noise on the blocker-rejection performance of the filter. Interestingly, it was shown that the differential part of the phase-noise in all the clock paths, to a first order, is not important and only the common-mode phase-noise does the reciprocal mixing. In summary, there are two problems associated with the existence of large blockers: 1) gain compression; and 2) reciprocal mixing. The first one is resolved by the exploitation of N-path filters. However, the latter remains a challenge.

- LO leakage can lead to an undesired tone in the case of a 3rd-order nonlinearity. The input signal located at $f_\mathrm{lo} + f_\mathrm{m}$ in conjunction with the LO leakage leads to an IM3 component located at $f_\mathrm{lo} - f_\mathrm{m}$. For asymmetrical modulations, this leads to the corruption of the received signal. It should be noted that the same undesired tone can be produced in the case of mismatch in the circuit. This issue and the severity of its implications needs to be addressed.

Acknowledgement

You embark on a Ph.D. with a passion of inventing world-changing ideas and revolutionizing your field of study. However, with the passage of time, you will realize that the only thing that is changing is you, hopefully in a good manner by gaining knowledge and expertise in your field.

From a course about integrated filter design, I was aware of an elegant yet simple approach to design high-frequency integrated filters by Prof. Bram Nauta. In my master thesis, I was working on low-noise amplifiers and after a few literature search, I confronted with a fascinating technique: "noise-canceling LNA", again by Prof. Nauta's group. In year 2009, the time that I was applying for a Ph.D. position abroad, ICD group had 5 papers at ISSCC conference, the foremost conference in the field of solid-state circuit design.[4] This was the best place for an ambitious person like me and therefore I emailed Prof. Nauta and fortunately I was admitted. After finishing my bachelor and master studies in Tehran, it was the time to go to Enschede to start my Ph.D. program. I thank him for giving me this opportunity. I was always amused by his intuitive method of thinking, his sharpness and his technical expertise.

My assistant-promoter, Dr. Ronan van der Zee, was no different. Most of the time, other than the assigned weekly-meeting hours, I could walk to his office and have a discussion with him. This was very crucial and helpful. He was open to discussions on very different topics. I do remember that one time, we were talking about the importance of generation of the α waves in the brain for the creation of new ideas. He was industrious and critical when giving countless feedbacks on different versions of our articles and this thesis which substantially improved their quality. Thank you, Ronan.

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[4]In 2012, we broke our record by having 8 accepted papers.

van Vliet. Although Dr. Eric Klumperink was not my direct supervisor, we had numerous fruitful discussions and collaborations. I would like to thank Michiel and Mark for their help during the measurements. Thanks as well go STW (Dutch Technology Foundation) for funding this project, STMicroelectronics for silicon donation and CMP for their assistance.

I enjoyed occasional coffee-break discussions with two of my friends, Behnam and Farhad, on different topics ranging from physics to movies. Interesting late evening discussions on circuit design with Shadi was almost like a tradition. I liked the discussions that I had with my office-mate, Saifullah, on the power converters. Also, he taught me how to fly a kite. In my project, I worked closely with two of my colleagues, Hadi (from TST group) and Naveed (from SC group). Initially, due to coming from different fields of studies namely electrical and mechanical engineering, we had difficulties in interpreting each other's sentences. Fortunately, consequently, we found a common language to talk and we had countless discussions on MEMS. These collaborations and discussions have led Hadi and I to publish some papers together. I would like to thank all my Iranian friends particularly Farhad, Elahe, Hadi, Behnam, Alireza, Zahra and Masumeh for the fun that we had together.

Without benefiting from having correct initial conditions[5], it would have been impossible to achieve what I have managed to achieve in my life. For this initial conditions namely providing good genes and up-bringing, I am deeply grateful to my parents.

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<div align="right">

Milad Darvishi
Enschede, August 2013

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[5]I assume that we, humans, are very complex PDEs.

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List of publications

[1] **M. Darvishi**, R. van der Zee, E. Klumperink, and B. Nauta, "A 0.3-to-1.2 GHz tunable 4th-order switched G_m-C bandpass filter with > 55 dB ultimate rejection and out-of-band IIP3 of $+29$ dBm," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* pp. $358 - 360$, Feb. 2012.

[2] **M. Darvishi**, R. van der Zee, E. Klumperink, and B. Nauta, "Widely Tunable 4th Order Switched G_m-C Band-Pass Filter Based on N-path Filters," in *IEEE J. Solid-State Circuits,* vol. 47, no. 12, pp. $3105 - 3119$, Dec. 2012. (**invited paper**)

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[4] H.Yagubizade, **M. Darvishi**, et al., "Pulsed-Laser Deposited $Pb(Zr_{0.52},Ti_{0.48})O_3$-on-Silicon Resonators with High-Stopband Rejection Using Feed-Through Cancellation," in *Applied Physics Letters,* 102(6), 063509, 2013.

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Biography

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